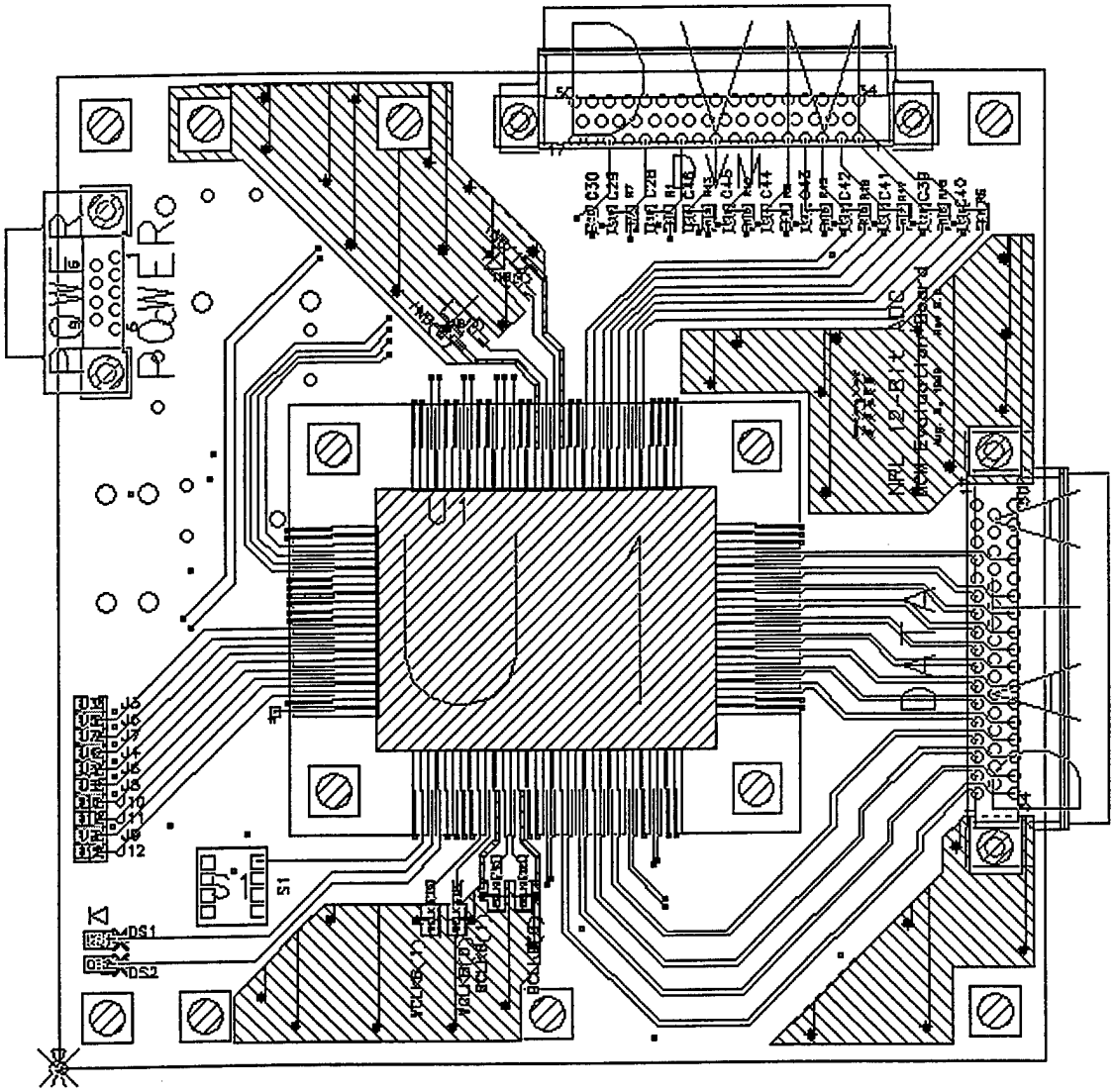
NRL 12-Bit, 213 Msps ADC
HSAD9 MCM Evaluation Board



December 8, 1999

Khanh Thai

Table of Contents

Table of Figures

Table of Tables

1. Evaluation Board Overview

The MCM Evaluation Board is a 6" by 6" test fixture designed for evaluating the HSAD9 MCM, a completely self-contained ADC multi-chip module that digitizes incoming differential analog signals to 12-bit resolution at a 213 Msps maximum sample rate. Data is output through a 50 pin D connector with LVDS logic levels. The MCM Evaluation Board functions very similarly to the AMAD19 12-bit ADC Breadboard. Its circuitry is very similar as well, with the major components that were once on the Breadboard now packaged on the HSAD9 MCM. The MCM is comprised of five major circuit blocks: the AMAD19 custom GaAs HBT circuit, a Calibration FPGA, a non-volatile Ram, two octal, 8-bit DACs, and reference generation circuitry. Many comparisons and references to the AMAD19 Breadboard document--1999-D502-020, "NRL 12-Bit, 213 Msps ADC Breadboard and Calibration FPGA," by T. Zylman and K. Thai--will be made throughout this document.

1.1. Block Diagram

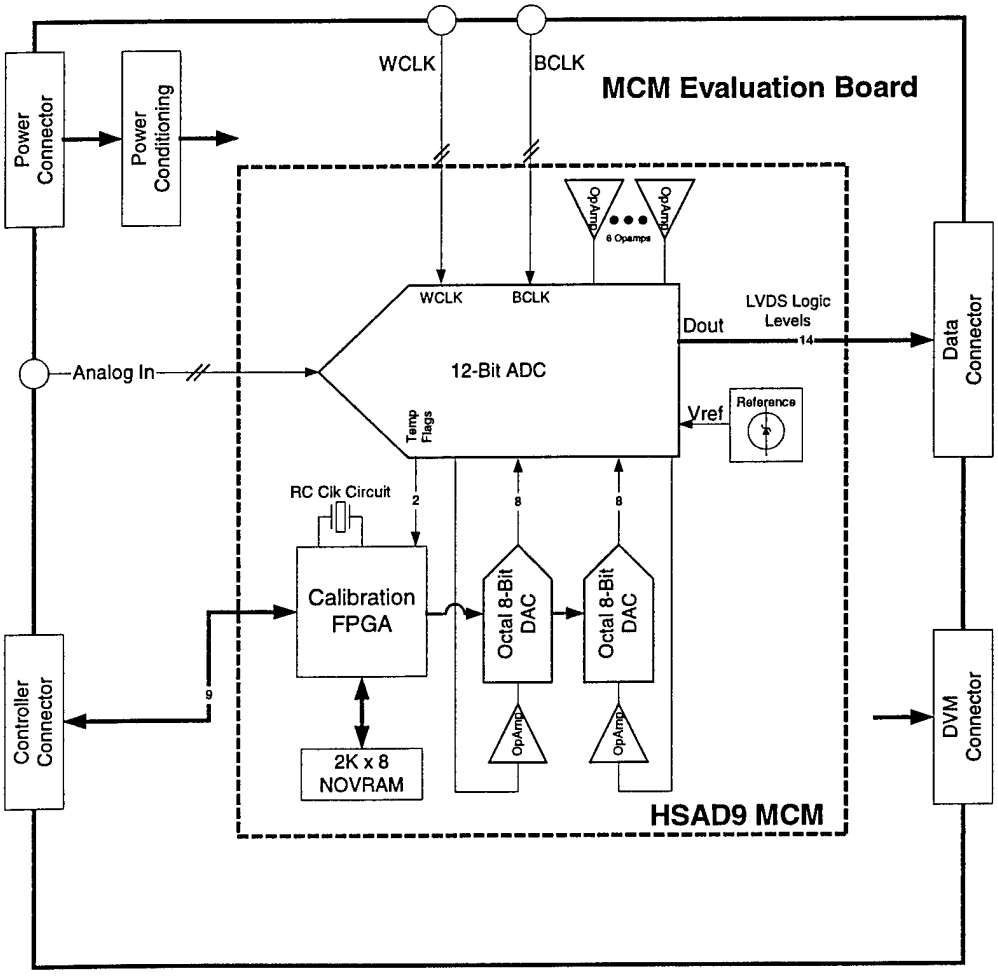


Figure 1-1: MCM Evaluation Board Block Diagram.

2. Evaluation Board Interfaces

Seven separate interfaces are provided on the Evaluation Board, and are described below.

2.1. Analog Interface

Differential analog input with SMA jack connectors on the edge of the Evaluation Board. Both sides of the differential signal are terminated with 50 Ω on the AMAD19 chip itself. See Figure 2-1. An optional phase splitter may be used to drive the ADC input differentially.

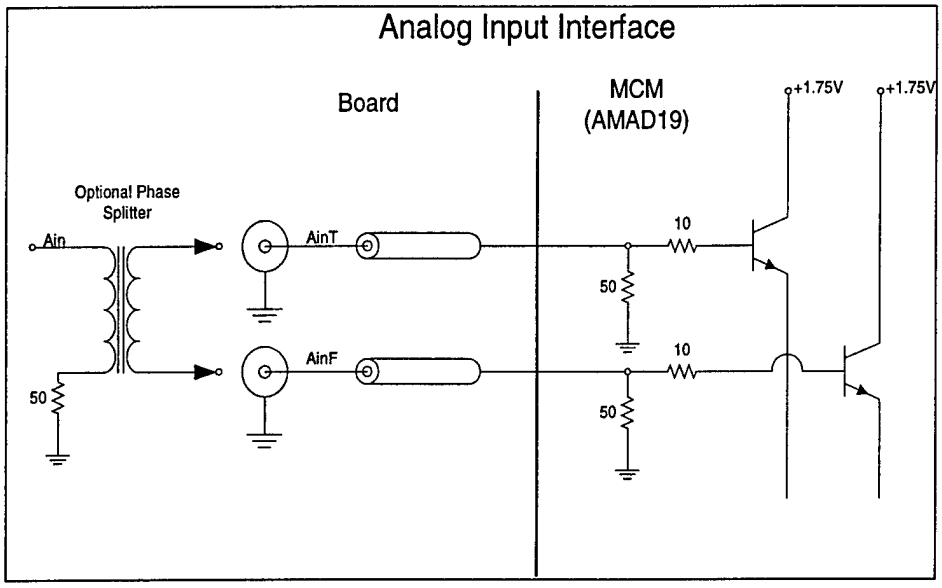


Figure 2-1: Analog Input Interface.

2.2. BClock Interface

Differential clock input with SMA jack connectors on the edge of the Evaluation Board. Both sides of the differential signal are terminated with 50 Ω on the AMAD19 chip itself. See Figure 2-2.

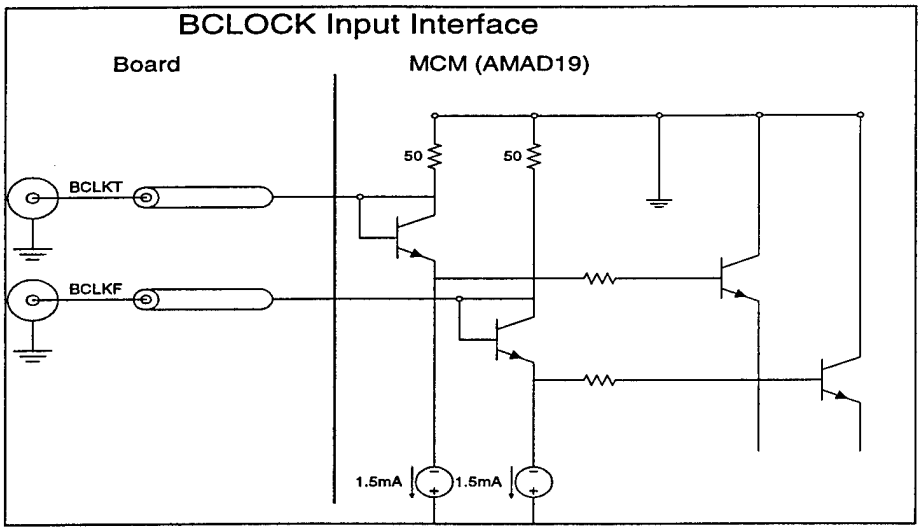


Figure 2-2: BCLOCK Interface.

2.3. WCLK Interface

Differential clock input with SMA jack connectors on the edge of the Evaluation Board. Both sides of the differential signal are optionally terminated with 50 Ω on the breadboard. See Figure 2-3. DC blocking capacitors are recommended on this port if driven by an external source.

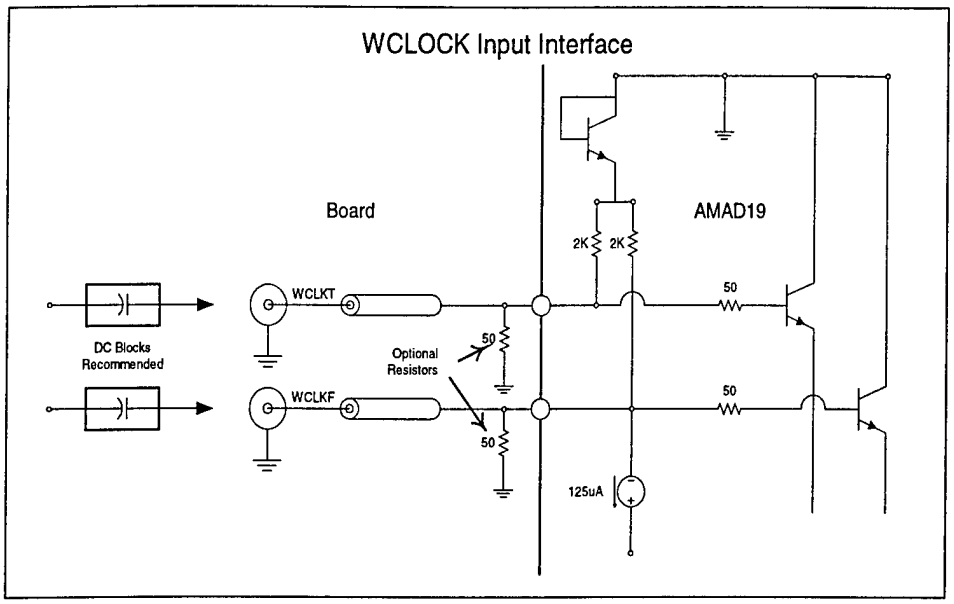


Figure 2-3: WCLK Interface.

2.4. ADC Data Interface

Figure 2-4 shows the LVDS interface circuit used for the ADC Data interface. Nominal logic levels for the LVDS interface are a common mode voltage of approximately 1.25V and a differential swing of about +/- 330 mV

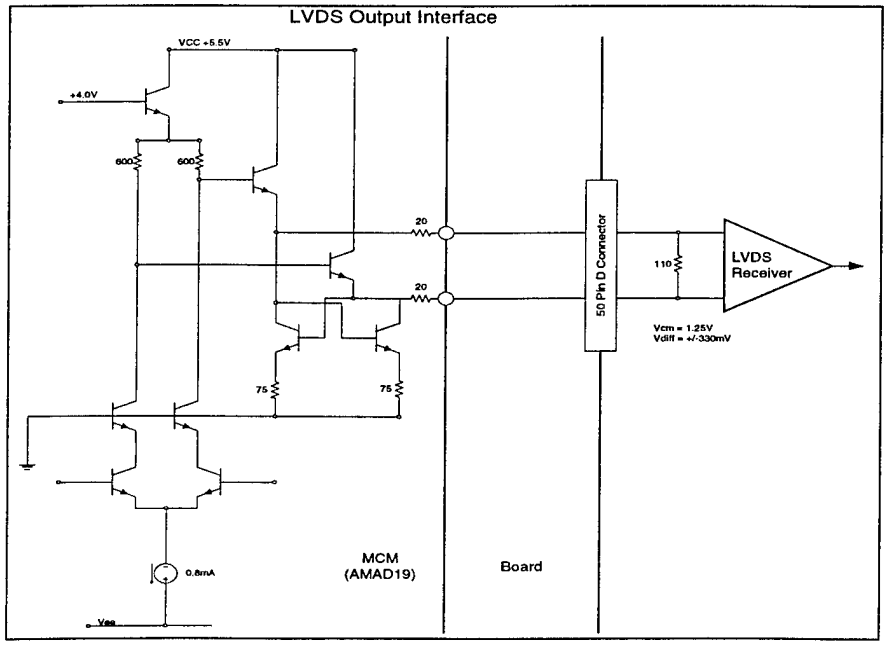


Figure 2-4 : Data Output Interface

Table 2-1 shows the pin assignment used in the 50 pin, female, D connector for the Data Output.

Table 2-1: Data Connector Pin Assignment.

Signal	Pin No	Signal	Pin No	Signal	Pin No
Q12T	1	GND	18	Q12F	34
Q11T	2	GND	19	Q11F	35
Q10T	3	GND	20	Q10F	36
Q9T	4	GND	21	Q9F	37
Q8T	5	GND	22	Q8F	38
Q7T	6	GND	23	Q7F	39
Q6T	7	GND	24	Q6F	40
Q5T	8	GND	25	Q5F	41
Q4T	9	GND	26	Q4F	42
Q3T	10	GND	27	Q3F	43
Q2T	11	GND	28	Q2F	44
Q1T	12	GND	29	Q1F	45
QF2T	13	GND	30	QF2F	46
QF1T	14	GND	31	QF1F	47
OVRT	15	GND	32	OVRF	48
Not Used	16	GND	33	Not Used	49
CLKOUTT	17			CLKOUTF	50

2.5. Controller Interface

A 20 pin, dual row header is used to interface the controller to the Evaluation Board. The pin assignment for this connector is shown in Table 2-2. All signals for this interface are TTL compatible.

Table 2-2: Controller Interface Connector Pin Assignment.

Signal	Pin No	Signal	Pin No
CSDO	1	GND	2
CSCLK	3	GND	4
CRESETN	5	GND	6
CSLDN	7	GND	8
CSDI	9	GND	10
CNE*	11	GND	12
CWE*	13	GND	14
CCE*	15	GND	16
COE*	17	GND	18
GND	19	GND	20

2.6. DVM Sense

A 50 pin, female D, connector is used for the DVM interface connector. Pinouts for this connector is shown in Table 2-33.

Table 2-3: DVM Sense Connector Pinout.

Signal	Pin No	Signal	Pin No	Signal	Pin No
DACREFM	1	GND	18	BSENP	34
WBAREFP	2	GND	19	BREFM	35
CMSENM	3	GND	20	DACSENP	36
TDACBUF	4	GND	21	WBASENM	37
RESENP	5	GND	22	CMREFP	38
LADSENP	6	GND	23	RESREFM	39
LADREFM	7	GND	24	Not Used	40
TEMPL	8	GND	25	Not Used	41
TEMPH	9	GND	26	Not Used	42
VCCD	10	GND	27	Not Used	43
M1OUT	11	GND	28	Not Used	44
M1	12	GND	29	Not Used	45
Vr_n59	13	GND	30	Not Used	46
MADCREF	14	GND	31	Not Used	47
FLAGL	15	GND	32	Not Used	48
FLAGH	16	GND	33	Not Used	49
Not Used	17			Not Used	50

2.7. Power

A 9 pin, female D, connector is used to bring power into the Evaluation Board. The pin assignment for this connector is shown in Table 2-4.

2.7.1. Connector Pinout

Table 2-4: Power Connector Pinout.

Pin No	Supply
1	Vee^-
2	Vee^- sense
3	Vee^+ sense
4	Vee^+
5	$Vcca^+$
6	$Vcca^+$ sense
7	$Vcca^-$ sense
8	$Vcca^-$
9	Not Used

2.7.2. Power consumption

Table 2-5: MCM Evaluation Board Power consumption.

Supply	Voltage	Static Current	Dynamic Current	Total Current	Max Power
Vee	-7.5 V ±5%	0.591 A		0.591 A	4.433 W
Vcca	+5.5 V ±5%	0.096 A		0.096 A	0.528 W
Vcc	+5.5 V ±5%	0.117 A		0.117 A	0.644 W
Vccd	+5.0V ±5%	0.027 A	0.038 A	0.065 A	0.325 W

2.8. Test Mode Select Dip Switch

A four-position DIP switch is used on the Evaluation Board to select the functional modes of the FPGA Calibration Logic and the DVM outputs. These switches are factory set, and are not user selectable

2.8.1. Temperature Logic Override – Sw1

Table 2-6: Temperature Logic Override Switch Settings.

SW1	Temp. Logic Disabled
0	NO
1	YES

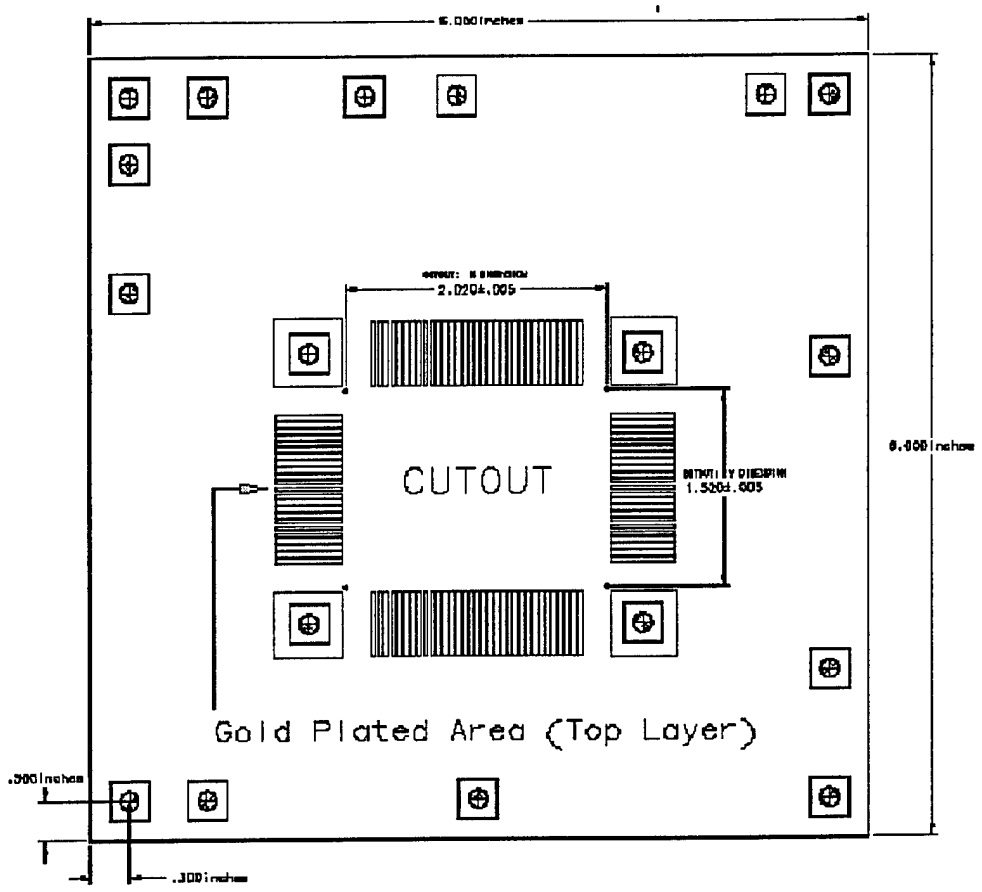
2.8.2. FlagL and FlagH DVM Sense Lines Control – Sw2 and Sw3

Table 2-7: S/H Override Switch Settings.

SW2 (FlagL)	SW3 (FlagH)	DVM Output
0 (open)	0 (open)	No Signal
1 (closed)	1 (closed)	Signal

2.8.3. Not Used – Sw4

2.9. Evaluation Board Mechanical Drawings



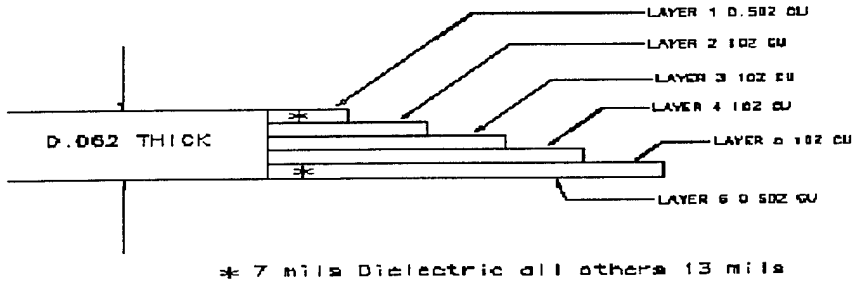


Figure 2-5: Evaluation Board Mechanical Dimensions.

2.10. Heatsink and Clamp.

A custom machined heatsink and clamp is used to dissipate the heat of the HSAD9 MCM and clamp it to the circuit board to provide a socket for testing multiple parts.

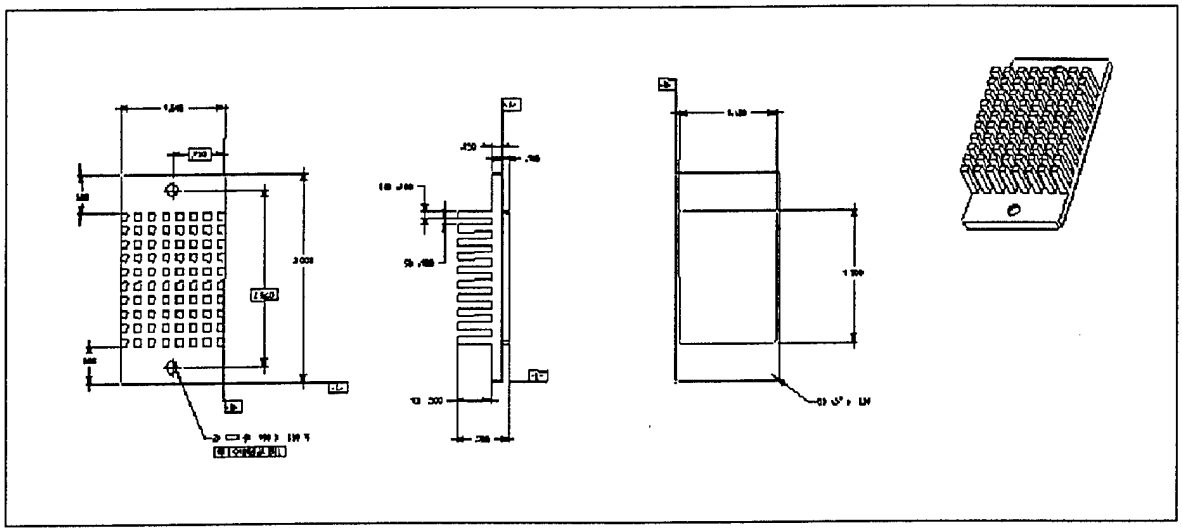


Figure 2-6: Heatsink Mechanical Drawing

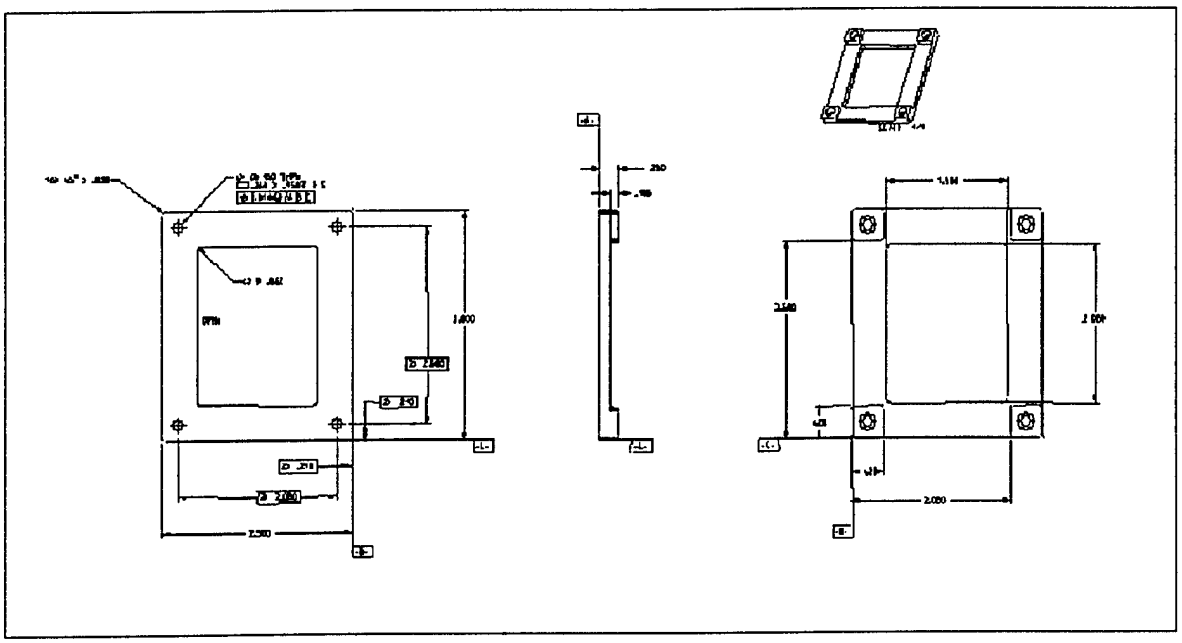


Figure 2-7: Top Clamp Mechanical Drawing.

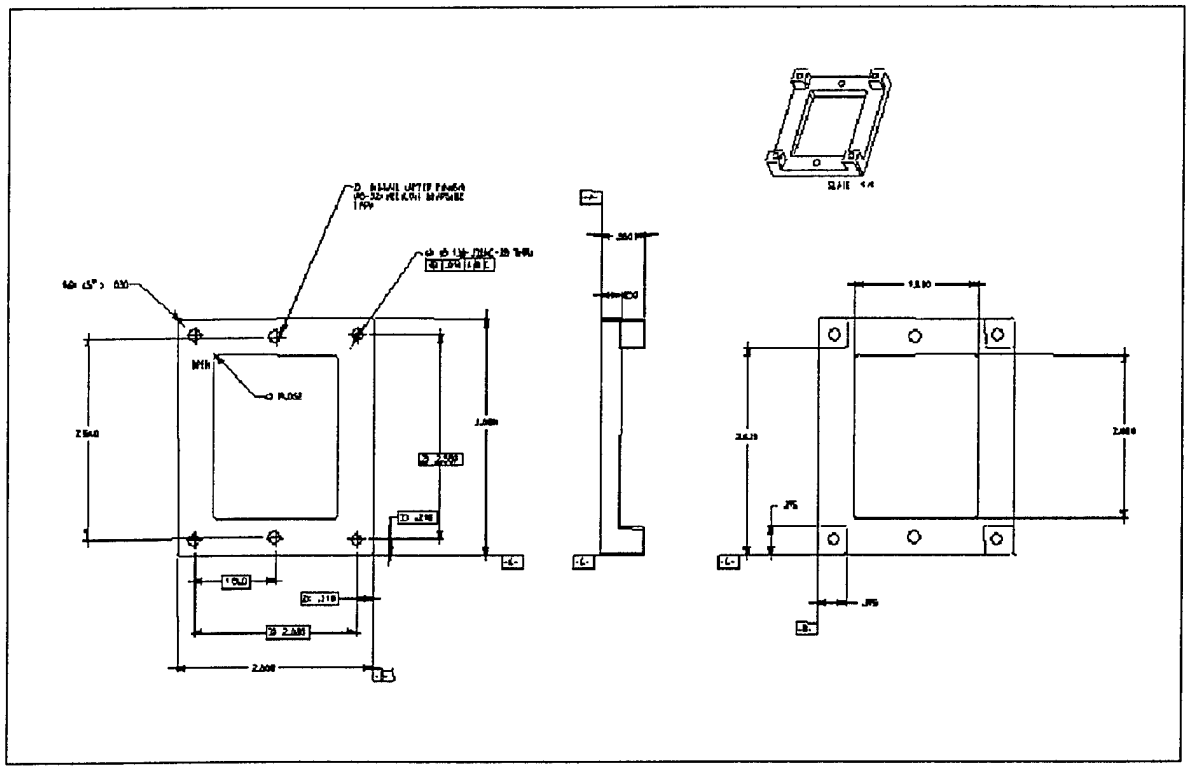


Figure 2-8: Bottom Clamp Mechanical Drawing.

3. HSAD9 MCM

The HSAD9 is a custom high temperature cofired ceramic multi-chip module built by NTK Ceramics. Figure 3-1 shows the MCM layout and pinouts. The 112-lead MCM is 1.5" by 2" and contains the AMAD19 12-Bit ADC (U8 in Fig. 3-1), an EEPROM (U9), an FPGA(U7), two Octal-DACs (U4 & U5), two Quad-Op-Amps (U1 & U2), and a voltage reference (VR1). Table 3-1 describes each pinout.

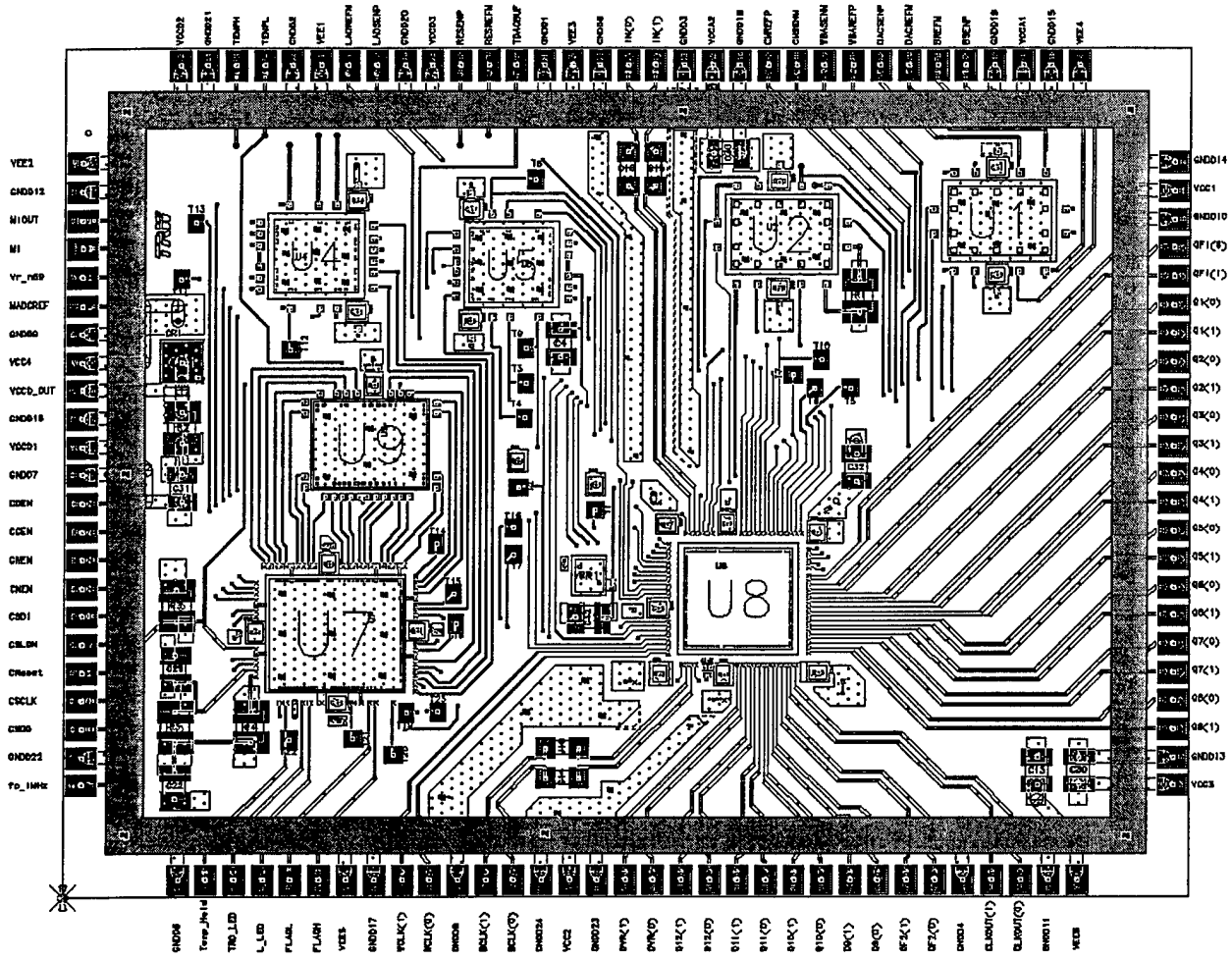


Figure 3-1: HSAD9 MCM Layout.

Table 3-1: HSAD9 MCM Pin Description.

Pin	Pin Name	Pin Description	Comments	Bias
1	VEE2			-7.5V
2	GNDD12			0V
3	M1out	DC Monitor	-1V internally generated from Madcref	-1V
4	M1		-1V opamp buffered version of M1out	-1V
5	Vr_n59		-5.9V Op Amp buffered version of TDACBUF	-5.9V
6	MADCref		External -1.235V reference	-1.23V
7	GNDD9			0V
8	VCC4			+5.5V
9	VCCD_OUT		+5.0V from +5.5V through dropping diode; route to external noise filter	+5.0V
10	GNDD16			0V
11	VCCD1		+5.0 V input from external noise filter	+5.0V
12	GNDD7			0V
13	COEN	Trim Computer	(Not Required by User)	TTL
14	CCEN	Interface		TTL
15	CWEN			TTL
16	CNEN			TTL
17	CSDI			TTL
18	CSLDN			TTL
19	Creset			TTL
20	CSCLK			TTL
21	CSDO			TTL
22	GNDD22			0V
23	fc_1MHz		Output from 1-MHz RC oscillator, clock for FPGA	TTL
24	GNDD5			0V
25	Temp_Hold		Temperature logic override: "1" to override	TTL
26	TRO_LED	Calibration Indicator	Temp Range Over LED	TTL
27	L_LED	Calibration Indicator	Temp Table Load LED	TTL
28	FlagL	Temperature Flag	TTL – temperature below TempL	TTL
29	FlagH	Temperature Flag	TTL – temperature above TempH	TTL
30	VEE5			-7.5V
31	GNDD17			0V
32	WCLK(1)	Word Clock	213 MHz for synchronizing multiple	-1.5V
33	WCLK(0)	(Optional)	ADCs, otherwise unused	-1.25V
34	GNDD8			0V
35	BCLK(1)	Master Clock, T	Connect to 50Ω single-ended sinewave	N/A
36	BCLK(0)	Master Clock, F	Terminate 50Ω to ground	N/A
37	GNDD24			0V
38	VCC2			+5.5V
39	GNDD23			0V
40	OVRT	Over-range Outputs	High when input is out of range	LVDS
41	OVRF			LVDS
42	Q12T	Data Outputs	100 Ohm Line to Line termination at load	LVDS
43	Q12F		Q12 is LSB	LVDS
44	Q11T			LVDS
45	Q11F			LVDS
46	Q10T			LVDS
47	Q10F			LVDS

Pin	Pin Name	Pin Description	Comments	Bias
48	Q9T	Data Outputs		LVDS
49	Q9F			LVDS
50	QF2T	Fine Trim Outputs	Fine Latch 2nd MSB (Factory Cal Only)	LVDS
51	QF2F			LVDS
52	GNDD4			0V
53	CLKOUTT	Clock Outputs		LVDS
54	CLKOUTF			LVDS
55	GNDD11			0V
56	VEE6			-7.5V
57	VCC3			+5.5V
58	GNDD13			0V
59	Q8T	Data Outputs		LVDS
60	Q8F			LVDS
61	Q7T			LVDS
62	Q7F			LVDS
63	Q6T			LVDS
64	Q6F			LVDS
65	Q5T			LVDS
66	Q5F			LVDS
67	Q4T			LVDS
68	Q4F			LVDS
69	Q3T			LVDS
70	Q3F			LVDS
71	Q2T			LVDS
72	Q2F			LVDS
73	Q1T		Q1 is MSB	LVDS
74	Q1F			LVDS
75	QF1T	Fine Trim Outputs	Fine Latch MSB (Factory Cal Only)	LVDS
76	QF1F			LVDS
77	GNDD10			0V
78	VCC1			+5.5V
79	GNDD14			0V
80	VEE4			-7.5V
81	GNDD15			0V
82	VCCA1			+5.5V
83	GNDD19			0V
84	Bsenp	Opamp Control Loops	Ref and Sense go to the inputs of the opamp	0.5V
85	Brefm	DC Monitor	a "p" suffix means the opamp plus input	0.5V
86	DACrefm		a "m" suffix means the opamp minus input	-0.5V
87	DACsenp		B is for Bridge balance	-0.5V
88	WBArefp		DAC is for DAC gain	-2V
89	WBAsenm		DAC gain is trimmed with DACref	-2V
90	CMsenm		WBA is for WBA common mode	-2.5V
91	CMrefp		CM is for DAC common mode	-2.5V
92	GNDD18			0V
93	VCCA2			+5.5V
94	GNDD3			0V
95	INT	Analog Input	Connect to external phase splitter	±0.5V

Pin	Pin Name	Pin Description	Comments	Bias
96	INF	Analog Input	Connect to external phase splitter	±0.5V
97	GNDD6			0V
98	VEE3			-7.5V
99	GNDD1			0V
100	TDACBUF	Trim DAC Ref Buffer	-5.9V from chip to opamp buffer to Trim DAC	-5.9V
101	RESrefm	Opamp Control Loops	RES is for Residue amplifier gain	-0.5V
102	RESsenp	DC Monitor		-0.5V
103	VCCD3			+5.0V
104	GNDD20			0V
105	LADsenp	Opamp Control Loops	LAD is for Quantizer ladder gain	-0.5V
106	LADrefm	DC Monitor	Quantizer gain is trimmed with LADref	-0.5V
107	VEE1			-7.5V
108	GNDD2			0V
109	TempL	Trip Low	Analog Low temperature trip voltage input (monitor)	-0.5V
110	TempH	Trip High	Analog High temperature trip voltage input (monitor)	-0.5V
111	GNDD21			0V
112	VCCD2			+5.0V

3.1. HSAD9 MCM Mechanical Drawings

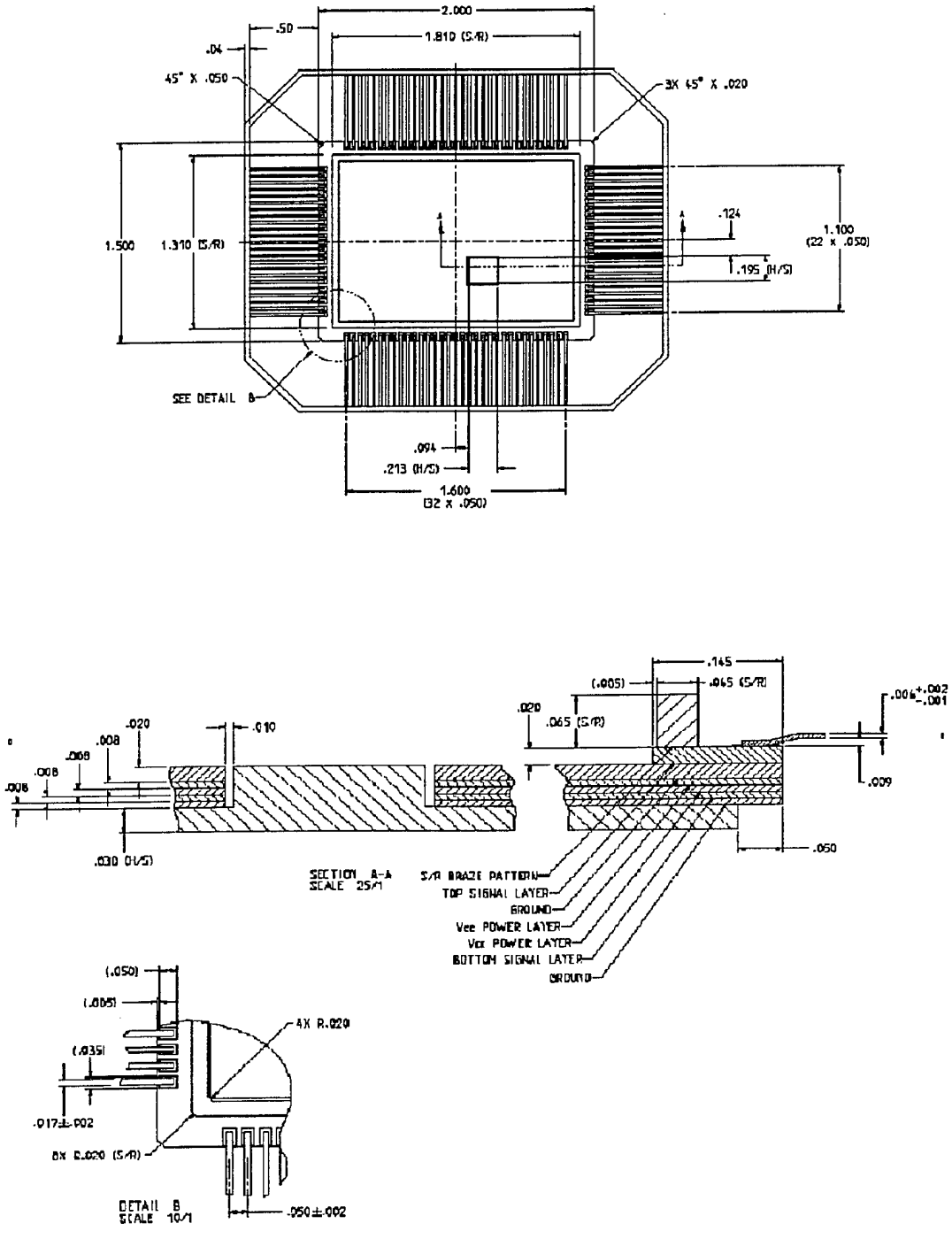


Figure 3-2: HSAD9 MCM Mechanical Dimensions.

3.2. AMAD19 – 12 Bit ADC

The AMAD19 is a 12-Bit, 213 Msps Analog-to-Digital Converter IC. It is designed and built by TRW in its GaAs HBT fabrication facility. Refer to ***Sections 3-1 and 3-2*** in the AMAD19 Breadboard document, 1999-D502-020, "NRL 12-Bit, 213 Msps ADC Breadboard and Calibration FPGA," by T. Zylman and K. Thai, for specifications and pin descriptions of the AMAD19.

3.3. DAC8800 – Octal DAC

Sixteen trim DACs are required to align and calibrate the AMAD19. Two Octal, Analog Devices, DAC8800's are used to perform this function. **Error! Reference source not found.** shows what the trim DACs are used for.

Table 3-2: TRIM DACs

Trim Point	# OF TRIM DACS	Resolution +/-	Range +/-	Comments
DAC Gain	1	1 LSB	5%	resolution at full scale
Quantizer Gain	1	.05 LSB	10%	resolution at full scale
RESAMP Gain	1	.08 LSB	175° C	range of compensation
C/F Offset	1	1.5 LSB	40 mV	referred to resamp input
DAC Level	8	.15 LSB	1.5%	1.5% of current source value
TEMP Limits	2	1.2° C	150° C	setting temperature threshold
Folder Offset	2	.03 LSB	8%	8% of folder bypass current
Total DACs	16			

The DAC's use a serial interface to reduce the pin count on the package. This interface is controlled via the calibration FPGA. Calibration coefficients are downloaded into the DACs during normal operation as temperature changes.

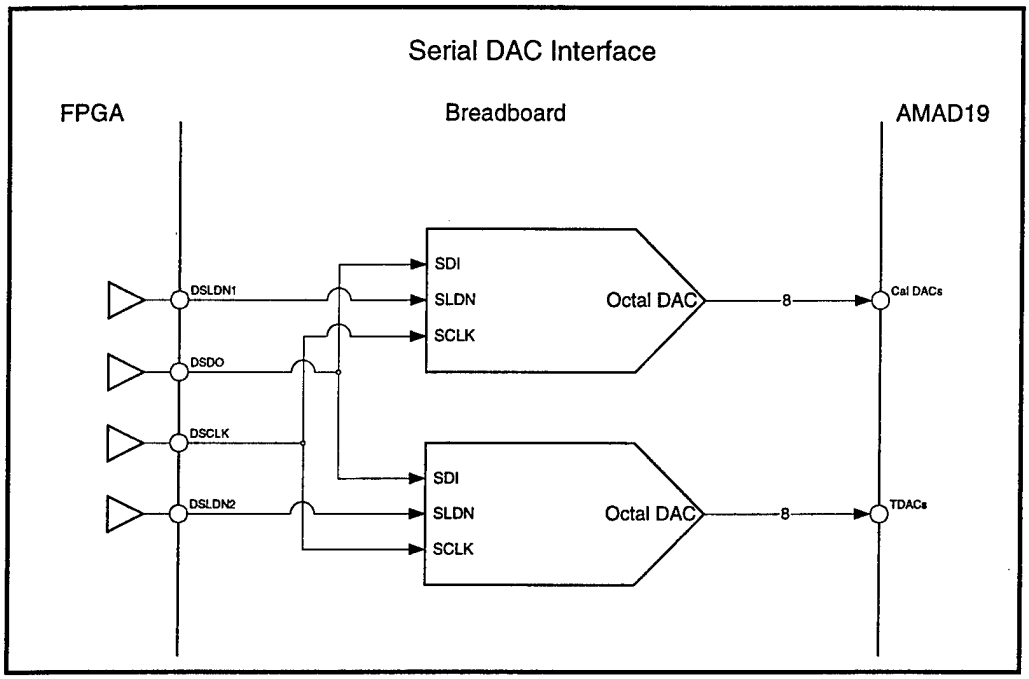


Figure 3-3: Calibration DAC Serial Interface.

Individual Trim DACs can be controlled via the computer interface by writing data to the EEPROM RAM as described in ***Section 5.2***, and then issuing a DAC Load command as described in ***Section 4.6.1*** in the AMAD19 Breadboard Document.

3.4. OP400 – Quad OpAmp

Two Analog Devices Quad Op-Amps, a total of eight op-amps, are used to buffer the signals to the ADC.

3.5. LM385 – 1.2V Voltage Reference

An external -1.235V reference is required for chip operation. The reference voltage is fed to the MADCREF input and divided down to –1V, and output on the M1out pin. The M1out signal is then buffered by an external opamp and fed back to the AMAD19 at the M1 input pin and also fed to one set of 8 external trim DACs as a low reference. This trim DAC uses a high reference input of 0 V and a low reference voltage of –1 V. SIT Resistors Rx and Rx may be used to adjust the –1 V value slightly.

A second voltage reference of about –5.9 V is output from the AMAD19 on the TDACBUF pin and buffered by an opamp. The buffered voltage is then fed to the second set of 8 DACs as its high reference input. This set of trim DACs uses VEE (-7.5 V) as its low side reference voltage. A SIT resistor may be installed on the opamp inverting terminal to VEE to adjust the reference voltage slightly.

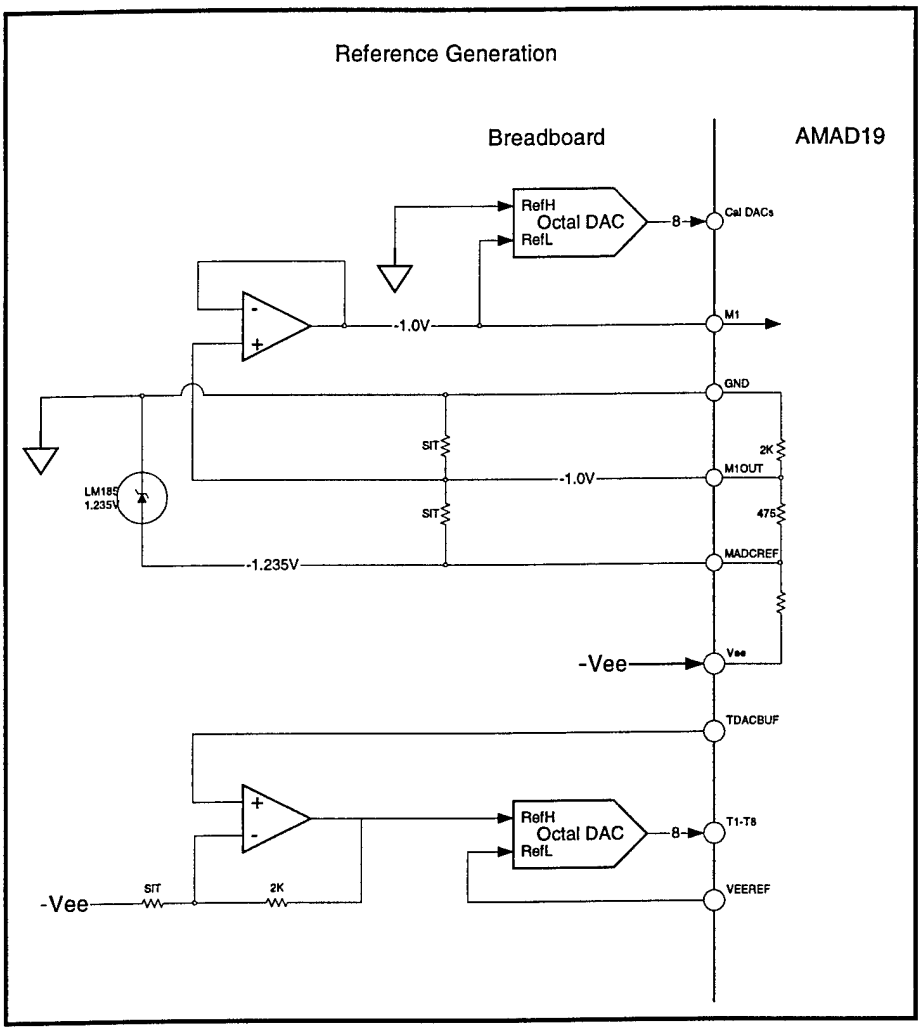


Figure 3-4: ADC Reference Generation.

3.6. A1225XL – Calibration FPGA

An ACTEL A1225XL FPGA is used to implement the Calibration Functions for the ADC. These functions include reading the current temperature of the ADC chip and detecting a change in temperature that requires a new set of calibration coefficients, reading calibration coefficients out of non-volatile memory, and downloading them to the calibration DACs. The FPGA also implements an interface to an external computer which allows control of the calibration functions, and a power on reset mode which defines the initial state of the ADC and calibration circuitry.

Figure 3-5 shows the block diagram for the calibration logic. The logic can be defined by seven unique blocks: a Controller Interface, Power On Reset Logic, Clock Logic, Temperature Logic, a non-Volatile Ram Interface, a Calibration DAC interface, and a Pulse Stretcher for an indicator light for Calibration Active.

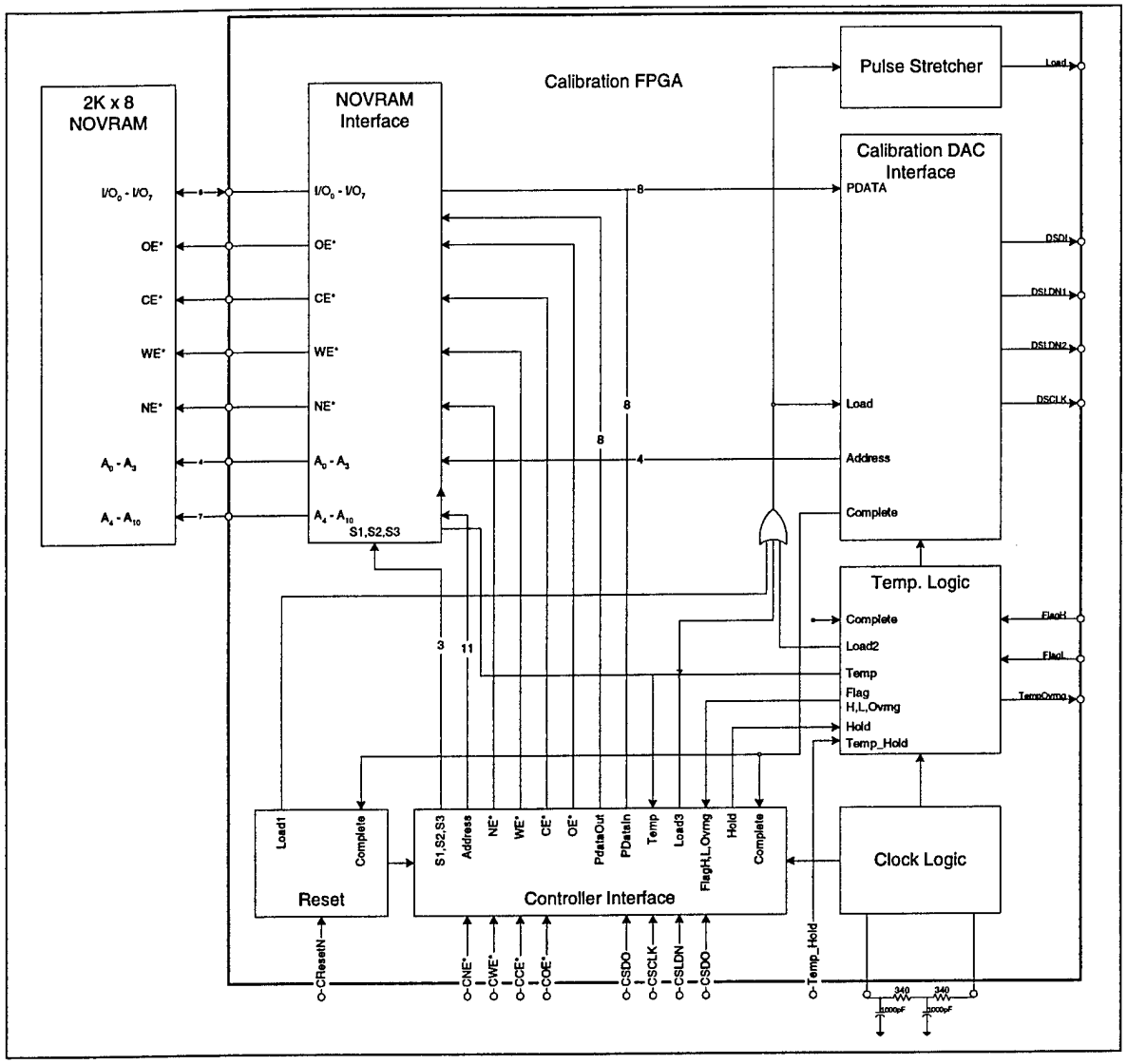


Figure 3-5: Calibration FPGA Block Diagram.

Refer to ***Section 4*** in the AMAD19 Breadboard document, 1999-D502-020, "NRL 12-Bit, 213 Msps ADC Breadboard and Calibration FPGA," by T. Zylman and K. Thai, to find details and functions of each of the unique blocks of the calibration circuitry. Several changes were made to the calibration circuitry for the FPGA on the HSAD9 MCM. An R-C clock circuit provides an external 2-MHz clock reference to the FPGA instead of the 16-MHz crystal. The Clock Logic now uses a D-Flip-Flop to divide the incoming clock signal down to the desired 1-MHz. Figure 3-10 shows the revised Clock Logic block. The Temp Logic was altered to program 31 temperature tables into the EEPROM instead of the 126. This will be detailed in the next section. Also, a Temp Logic disable pin was installed for manual override. These changes do not affect the existing user interface described in the AMAD19 Breadboard document.

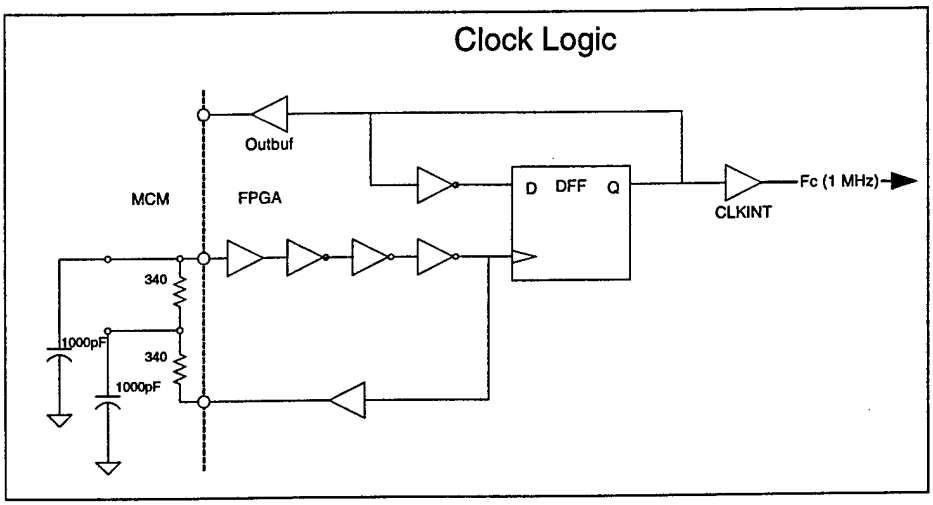


Figure 3-6: Revised Clock Logic Block Diagram.

3.7. X20C16 – EEPROM

An Electrically-Erasable-Programmable-Read-Only-Memory (EEPROM) with a built in shadow RAM (or NOVRAM for Non-Volatile RAM) is used to store calibration DAC codes for the ADC. The RAM is a 2K x 8, X20C16 from Xicor. For the EEPROM write and store commands, refer to ***Sections 5.2 and 5.3*** in the AMAD19 Breadboard document.

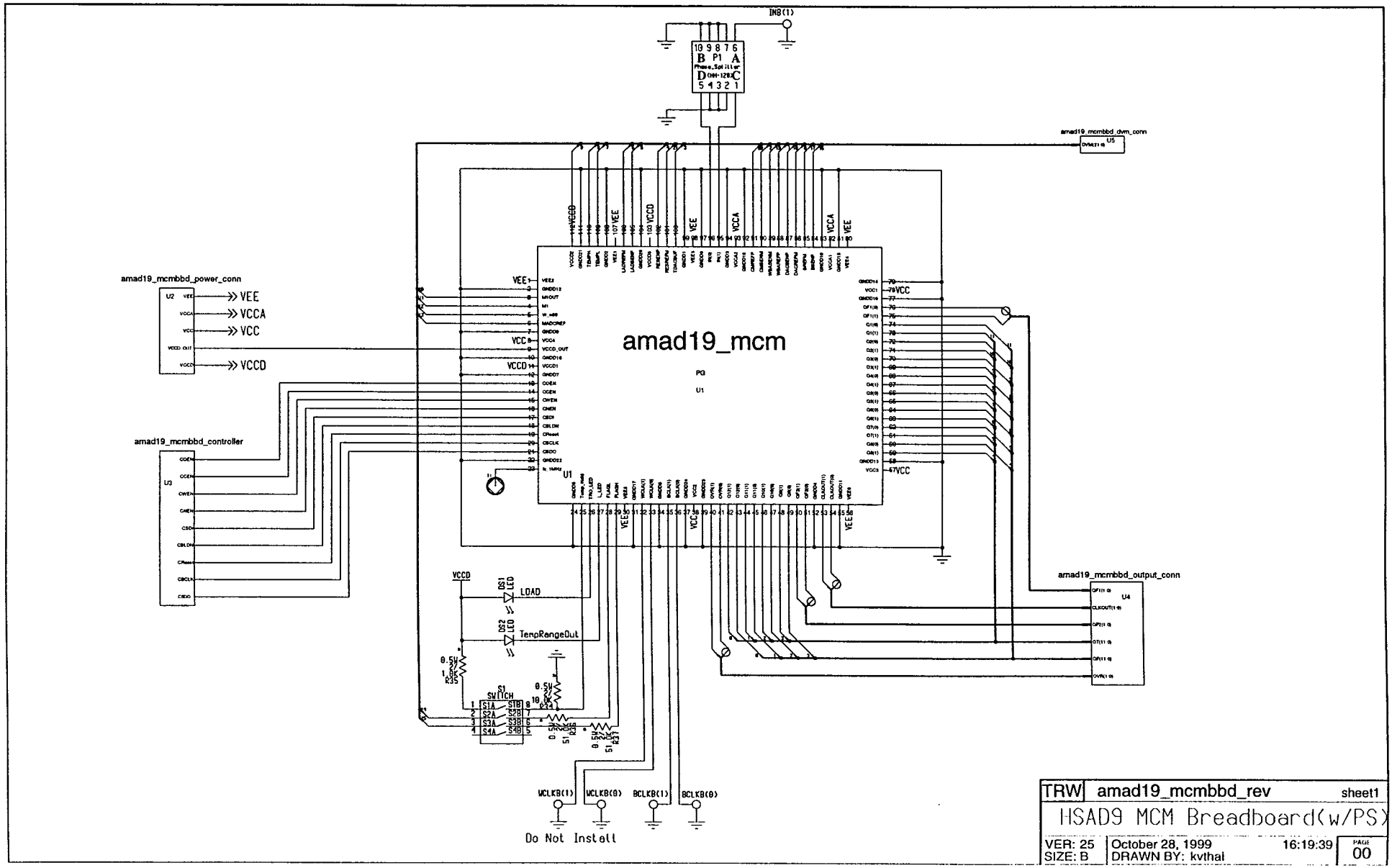
As mentioned in the previous section, there are 31 unique temperature tables stored in the EEPROM, each with 16 DAC word storage locations. Each DAC word is an 8-bit word. Two of the DAC locations are used for the temperature trip points – TempH and TempL. These two Memory locations must be preprogrammed in each of the 31 temperature tables before the temperature logic will function. Data is stored in the EEPROM as shown in Table 3-33.

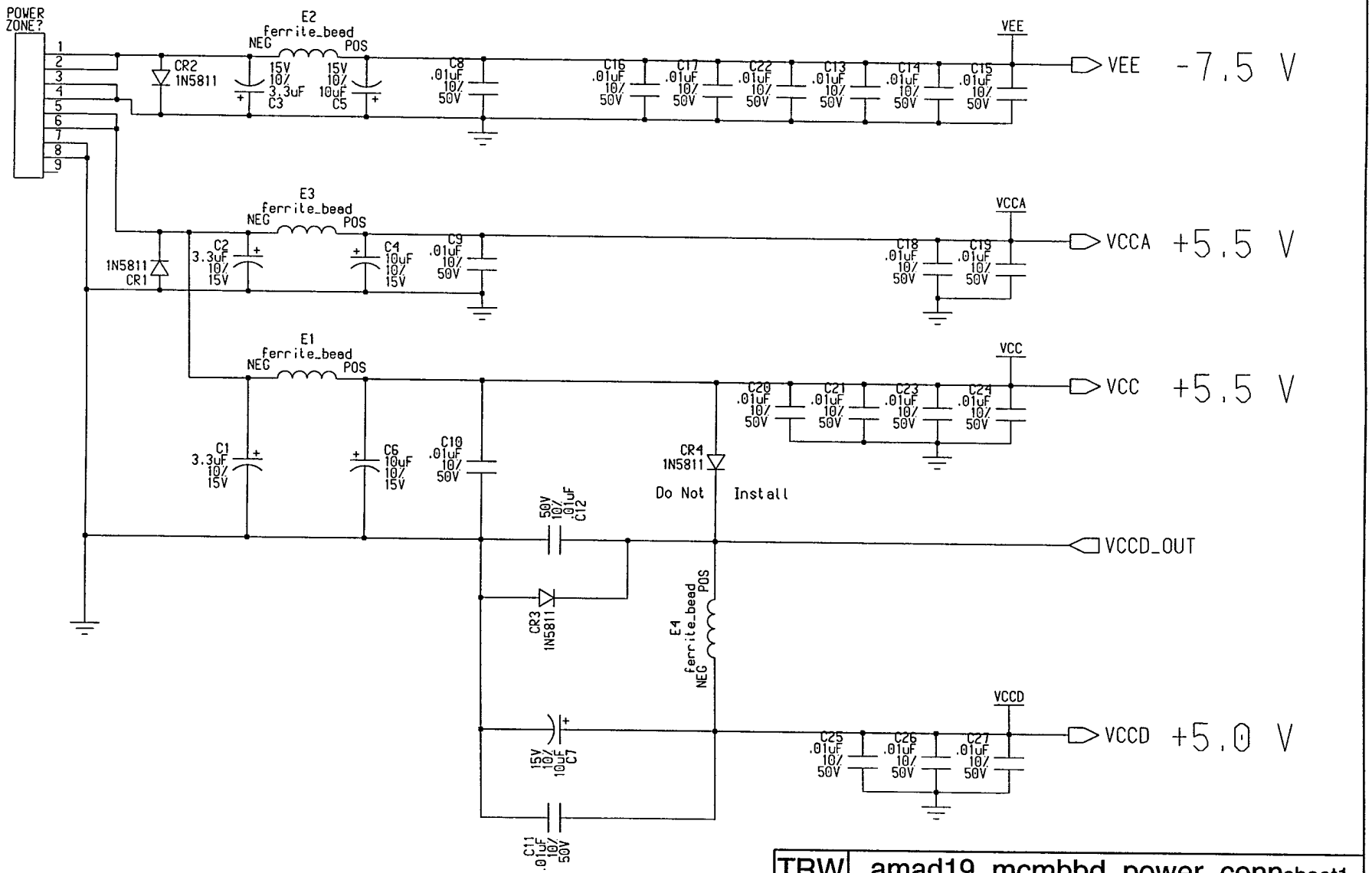
Table 3-3: EEPROM Memory Configuration.

NOVRAM Address			DAC Reference		
A10 – A0	Temp Bus A10 – A4	DAC Addr A3 – A0	DAC #	Name	Code
0#H	0	0	DAC 1 - 0	Ioffset	XXX
1#H	0	1	DAC 1 - 1	Qoffset	XXX
2#H	0	2	DAC 1 – 2	DACREFM	XXX
3#H	0	3	DAC 1 – 3	LADREFM	XXX
4#H	0	4	DAC 1 – 4	RESREFM	XXX
5#H	0	5	DAC 1 – 5	TempL	0
6#H	0	6	DAC 1 – 6	TempH	16
7#H	0	7	DAC 1 – 7	COFFT	XXX
8#H	0	8	DAC 2 – 0	T1	XXX
9#H	0	9	DAC 2 – 1	T2	XXX
A#H	0	10	DAC 2 – 2	T3	XXX
B#H	0	11	DAC 2 – 3	T4	XXX
C#H	0	12	DAC 2 – 4	T5	XXX
D#H	0	13	DAC 2 – 5	T6	XXX
E#H	0	14	DAC 2 – 6	T7	XXX
F#H	0	15	DAC 2 - 7	T8	XXX

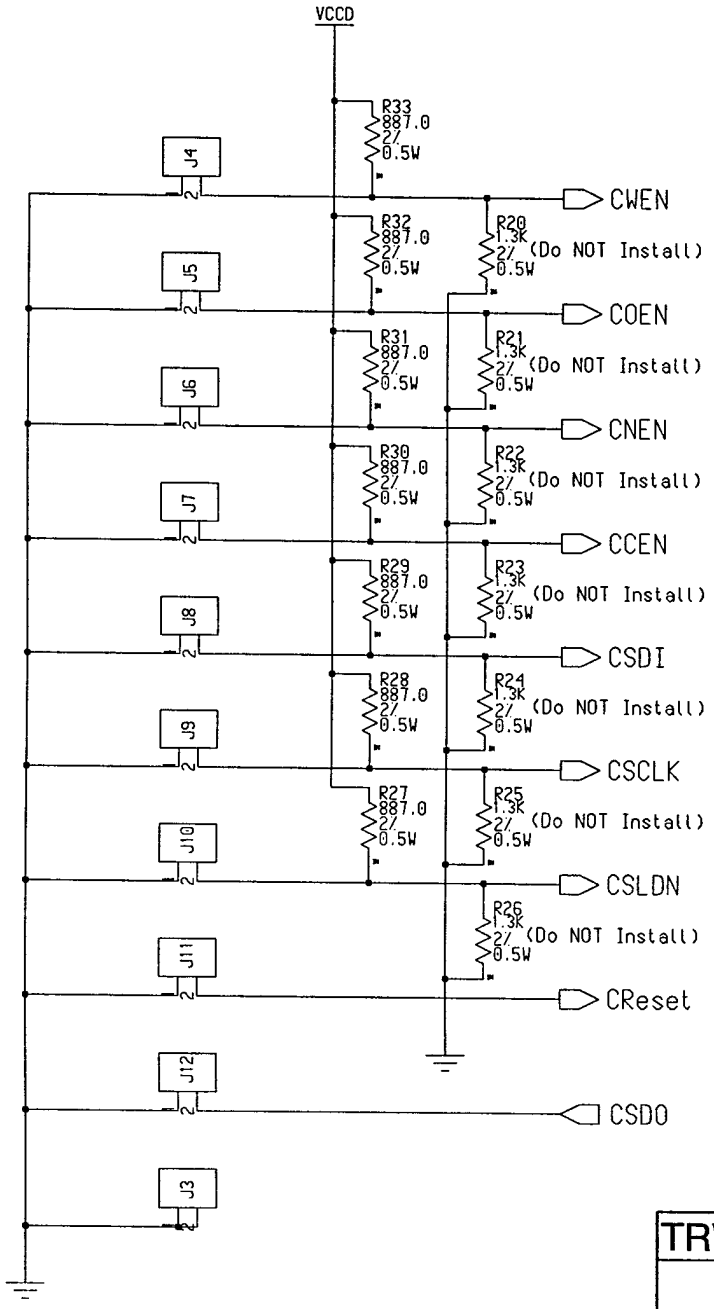
NOVRAM Address			DAC Reference		
A10 – A0	Temp Bus A10 – A4	DAC Addr A3 – A0	DAC #	Name	Code
40#H	4	0	DAC 1 - 0	Ioffset	XXX
•	•	•	•	•	•
45#H	4	5	DAC 1 – 5	TempL	8
46#H	4	6	DAC 1 – 6	TempH	24
•	•	•	•	•	•
4F#H	4	15	DAC2 – 7	T(8)	XXX
80#H	8	0	DAC 1 – 0	Ioffset	XXX
•	•	•	•	•	•
85#H	8	5	DAC 1 – 5	TempL	16
86#H	8	6	DAC 1 - 6	TempH	32
•	•	•	•	•	•
8F#H	8	15	DAC 2 –7	T(8)	XXX
C0#H	12	0	DAC 1 – 0	Ioffset	XXX
•	•	•	•	•	•
C5#H	12	5	DAC 1 – 5	TempL	24
C6#H	12	6	DAC 1 - 6	TempH	40
•	•	•	•	•	•
CF#H	12	15	DAC 2 –7	T(8)	XXX
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
740#H	116	0	DAC 1 - 0	Ioffset	XXX
•	•	•	•	•	•
745#H	116	5	DAC 1 – 5	TempL	232
746#H	116	6	DAC 1 - 6	TempH	248
•	•	•	•	•	•
74F#H	116	15	DAC 2 – 7	T(8)	XXX
780#H	120	0	DAC 1 - 0	Ioffset	XXX
•	•	•	•	•	•
785#H	120	5	DAC 1 – 5	TempL	240
786#H	120	6	DAC 1 - 6	TempH	255
•	•	•	•	•	•
78F#H	120	15	DAC 2 – 7	T(8)	XXX
7C0#H	120	0			Not Used
•	•	•	•	•	•
•	•	•	•	•	•
7CF#H	124	15			Not Used

4. Breadboard Schematics

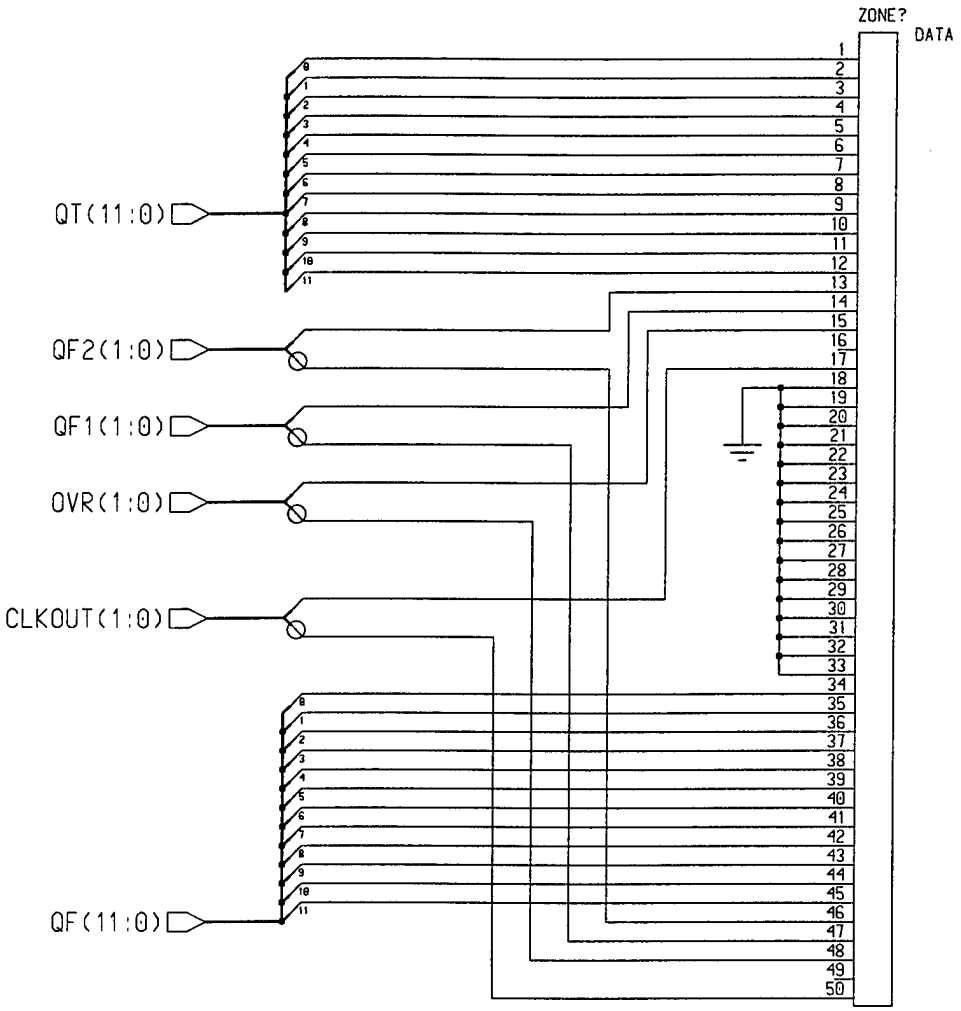

amad19_mcm
PG
U1
amad19_mcmbbd_power_conn
amad19_mcmbbd_controller
amad19_mcmbbd_output_conn
amad19_mcmbbd_dvm_conn
VEE
VCCA
VCC
VCCD
LOAD
TempRangeOut
Do Not Install
TRW amad19_mcmbbd_rev sheet1
HSAD9 MCM Breadboard(w/PS)
VER: 25
SIZE: B
October 28, 1999
DRAWN BY: kvthal
16:19:39
PAGE 00



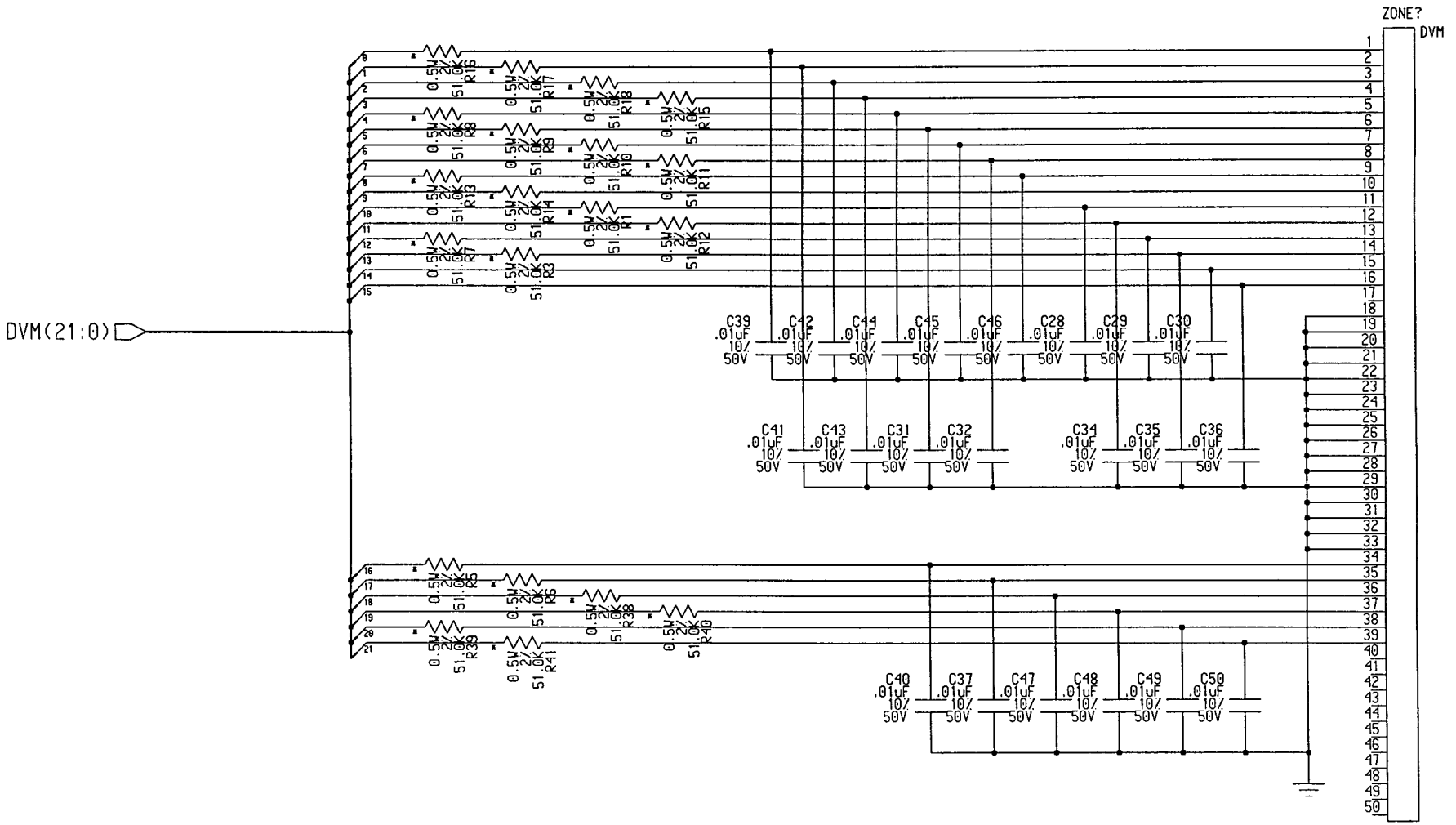
TRW	amad19_mcmbbd_power_conn	sheet1
VER: 7 SIZE: A	July 27, 1999 DRAWN BY: kvthai	09:49:49
		PAGE 00



TRW	amad19_mcmbbd_controller	sheet1
VER: 1 SIZE: A	July 12, 1999 DRAWN BY: kvthai	14:12:20
		PAGE 00



TRW	amad19_mcmbbd_output_conn sheet1		
VER: 3 SIZE: A	July 27, 1999 DRAWN BY: kvthai	09:49:21	PAGE 00



TRW	amad19_mcmbbd_dvm_conn	sheet1	
VER: 7 SIZE: A	August 26, 1999 DRAWN BY: kvthai	15:16:51	PAGE 00

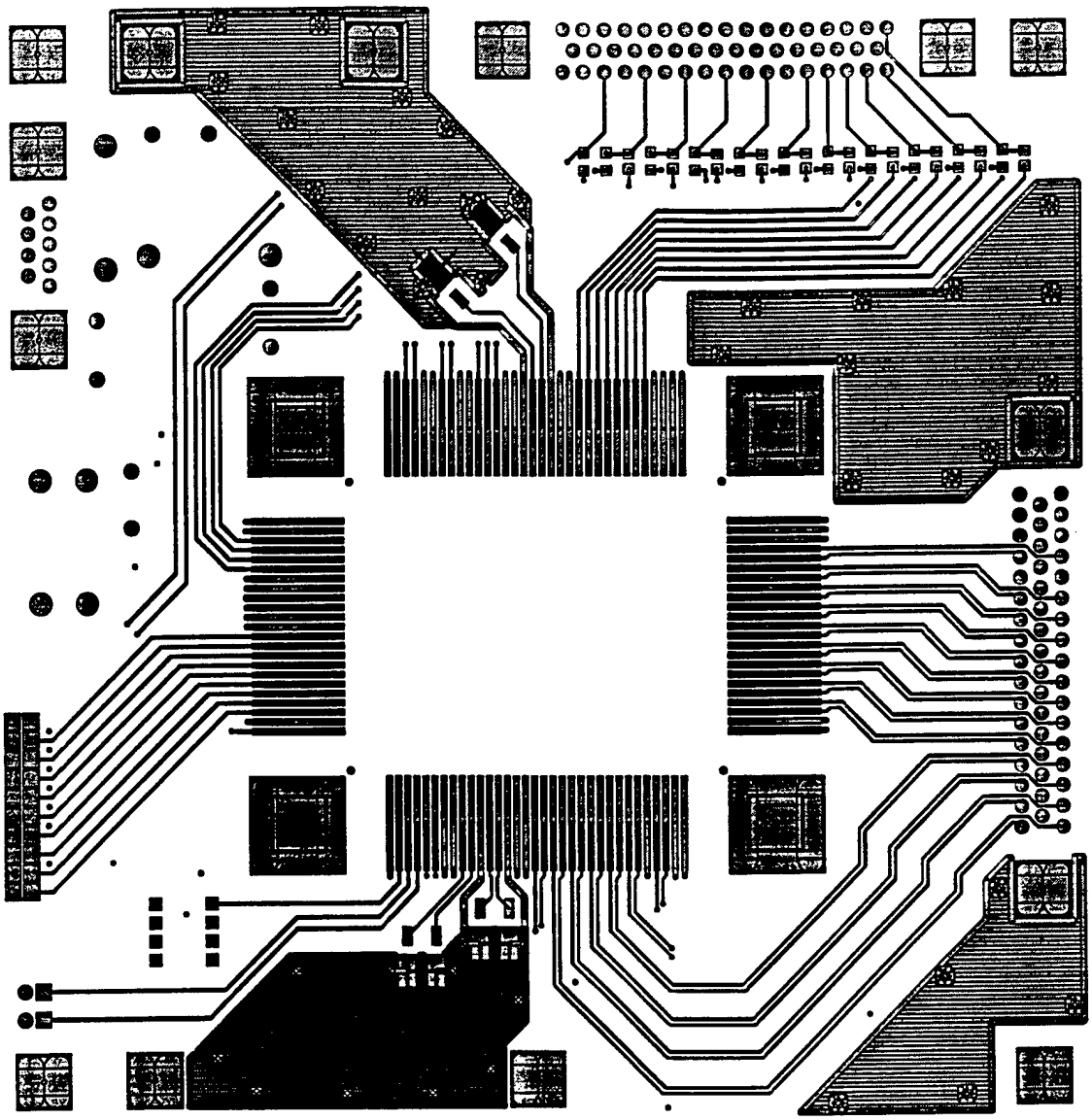
5. Bill of Material

Board Station BOM file

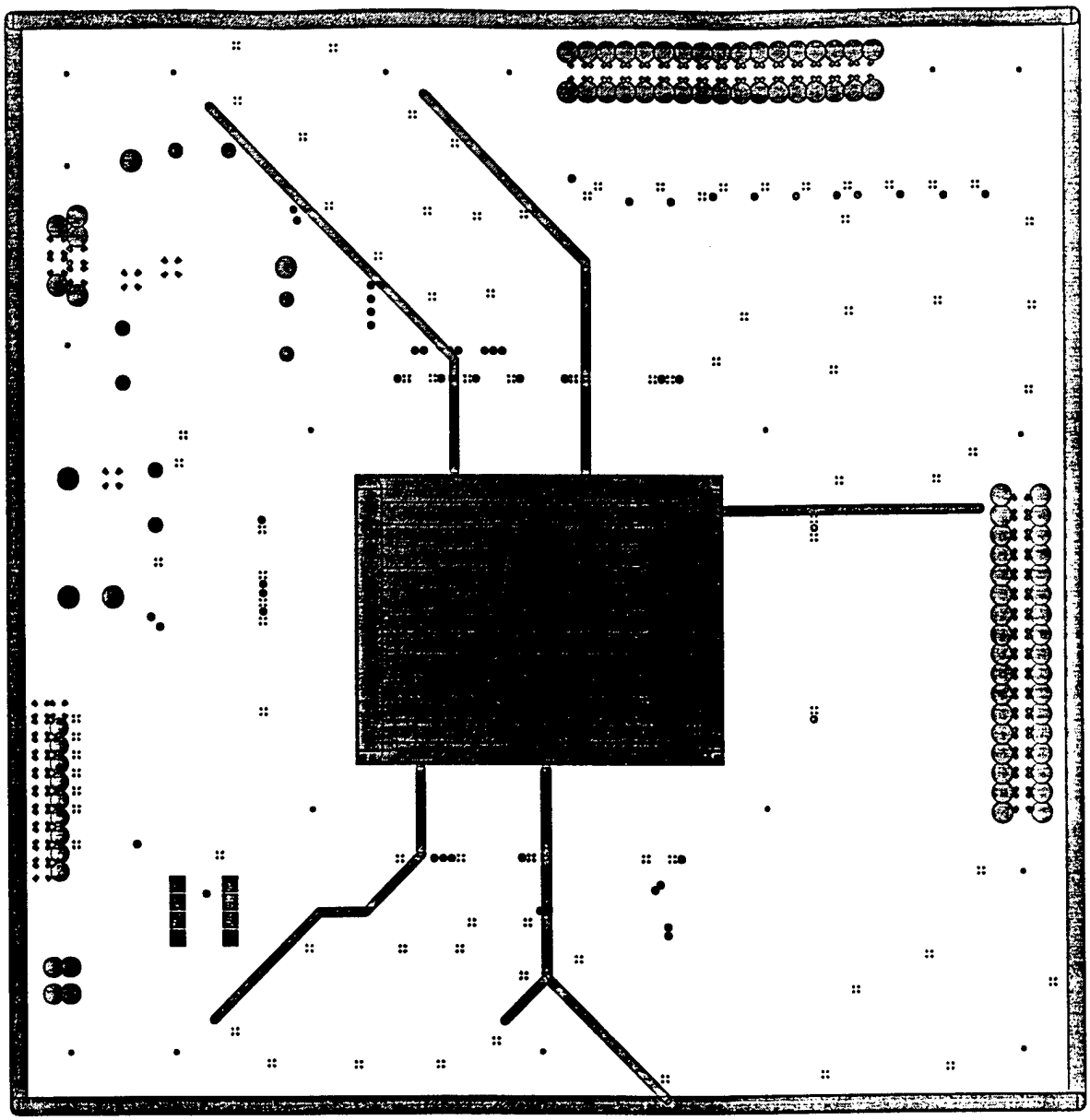
Tuesday August 31, 1999; 18:10:17

ITEM_NUMBER	PART NO.	ALT. PART NO.	COUNT	DESCRIPTION	REFERENCE	SOURCE
1	17D-D-50-P-AJ4	MD50F5R8NT2X	2	CONN 50p d-sub(fem)	DATA DVM	Positronic
2	1A036-337	PCC103BNCT-ND	41	CAP (0.01uF)	C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C34 C35 C36 C37 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50	Digi-Key
3	1A060-009	PCT3335CT-ND	3	CAP (3.3uF)	C1 C2 C3	Digi-Key
4	1A077-030	PCT5106CT-ND	4	CAP (10uF)	C4 C5 C6 C7	Digi-Key
5	1DA29-002	6A2DICT-ND	4	DIODE 1N5811	CR1 CR2 CR3 CR4	Digi-Key
6	1K070-070	P887CCT-ND	7	RES (887)	R27 R28 R29 R30 R31 R32 R33	Digi-Key
7	1K070-073	P1.00KCCT-ND	1	RES(1K)	R35	Digi-Key
8	1K070-097	P10.0KCCT-ND	1	RES(10K)	R34	Digi-Key
9	1K070-114	P51.1KCCT-ND	22	RES (51K)	R1 R3 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R36 R37 R38 R39 R40 R41	Digi-Key
10	1K070-124	P1.30KCCT-ND	7	RES (1.3K)	R20 R21 R22 R23 R24 R25 R26	Digi-Key
11	2643002402	P9820BK-ND	4	ferrite_bead	E1 E2 E3 E4	Digi-Key
12	555-2009	160-1045-ND (53-ND)	2	LED Red (Yellow)	DS1 DS2	Digi-Key
13	AMP747250-4	MD9F5R8NT2X	1	CONN 9p d-sub(fem)	POWER	Positronic
14	DP-04	CKN3003-ND	1	SWITCH dip4	S1	Digi-Key
15	PADS_FOR_COAX		6	PADS	BCLKB(0) BCLKB(1) INB(0) INB(1) WCLKB(0) WCLKB(1)	
16	TSW-102-08-S-S	S2011-36-ND	10	CONN Dual row 10p	J3 J4 J5 J6 J7 J8 J9 J10 J11 J12	Digi-Key
17	amad19_mcm		1	amad19_mcm	U1	TRW Inc.
18	probe_pad		1	probe_pad	T1	

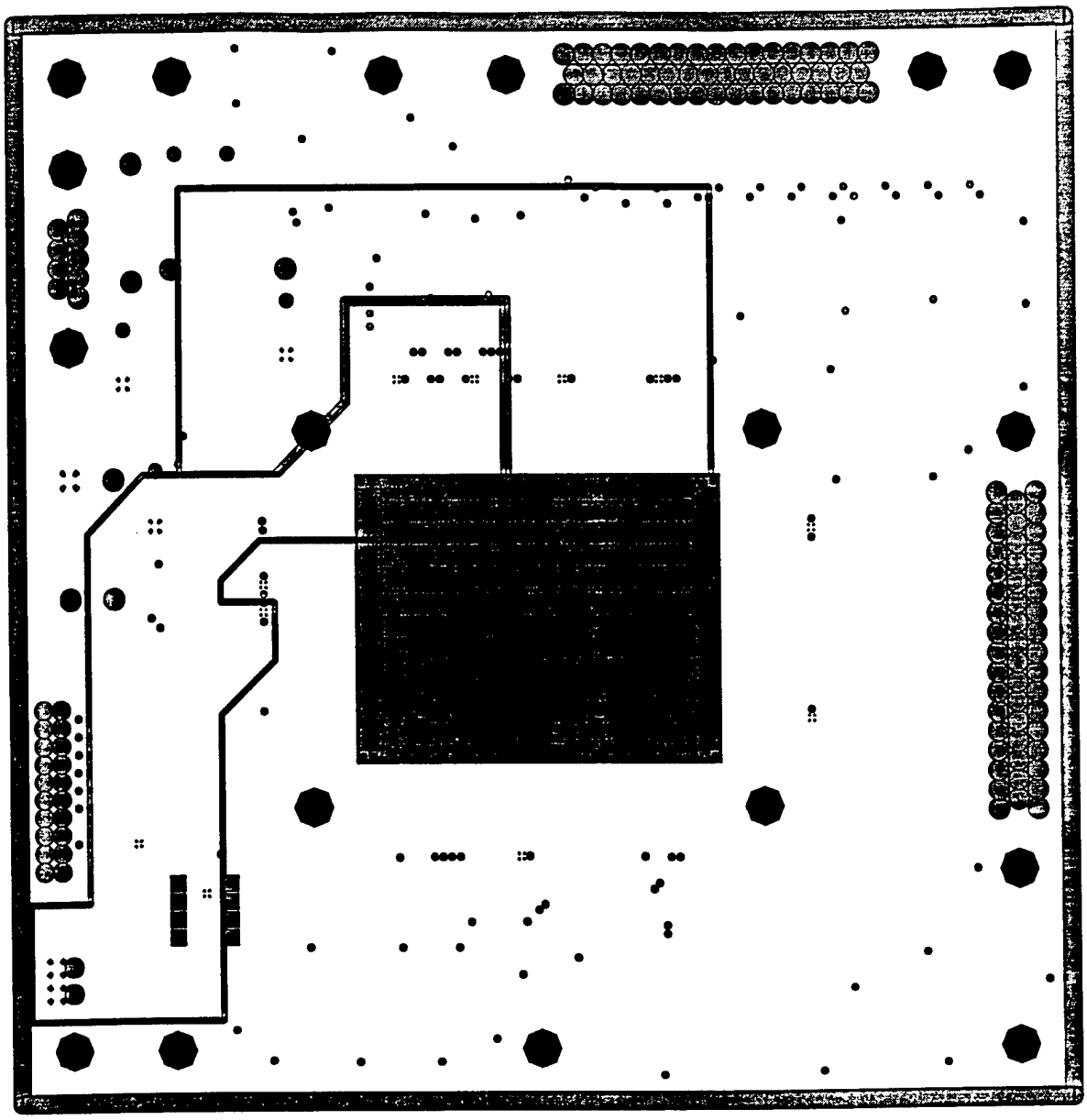
6. Breadboard Layout Plots



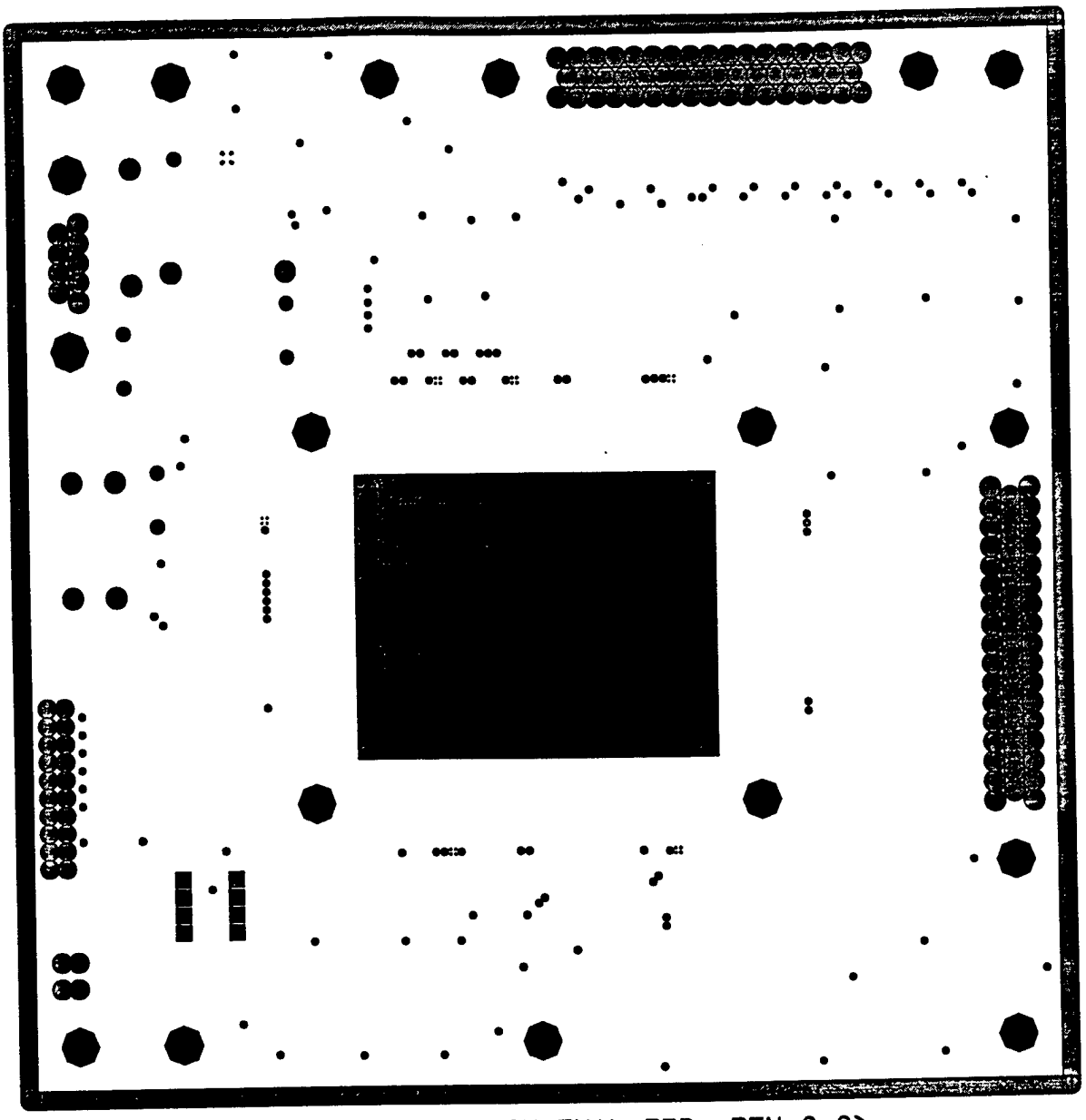
LAYER_1: SIGNAL_1 (NRL MCM EVAL BRD REV 0.0)



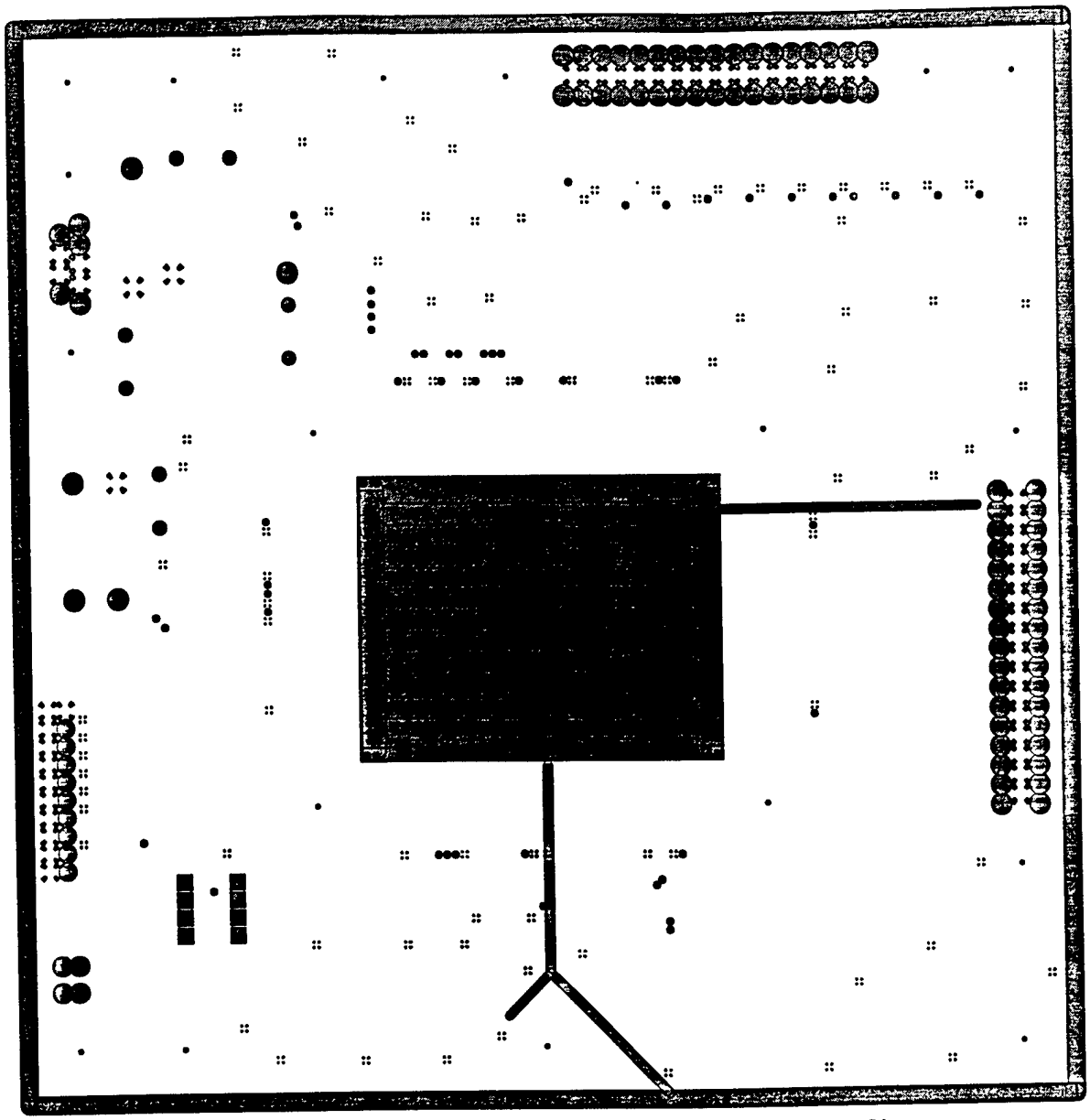
LAYER_2: GROUND (NRL MCM EVAL BRD REV 0.0)



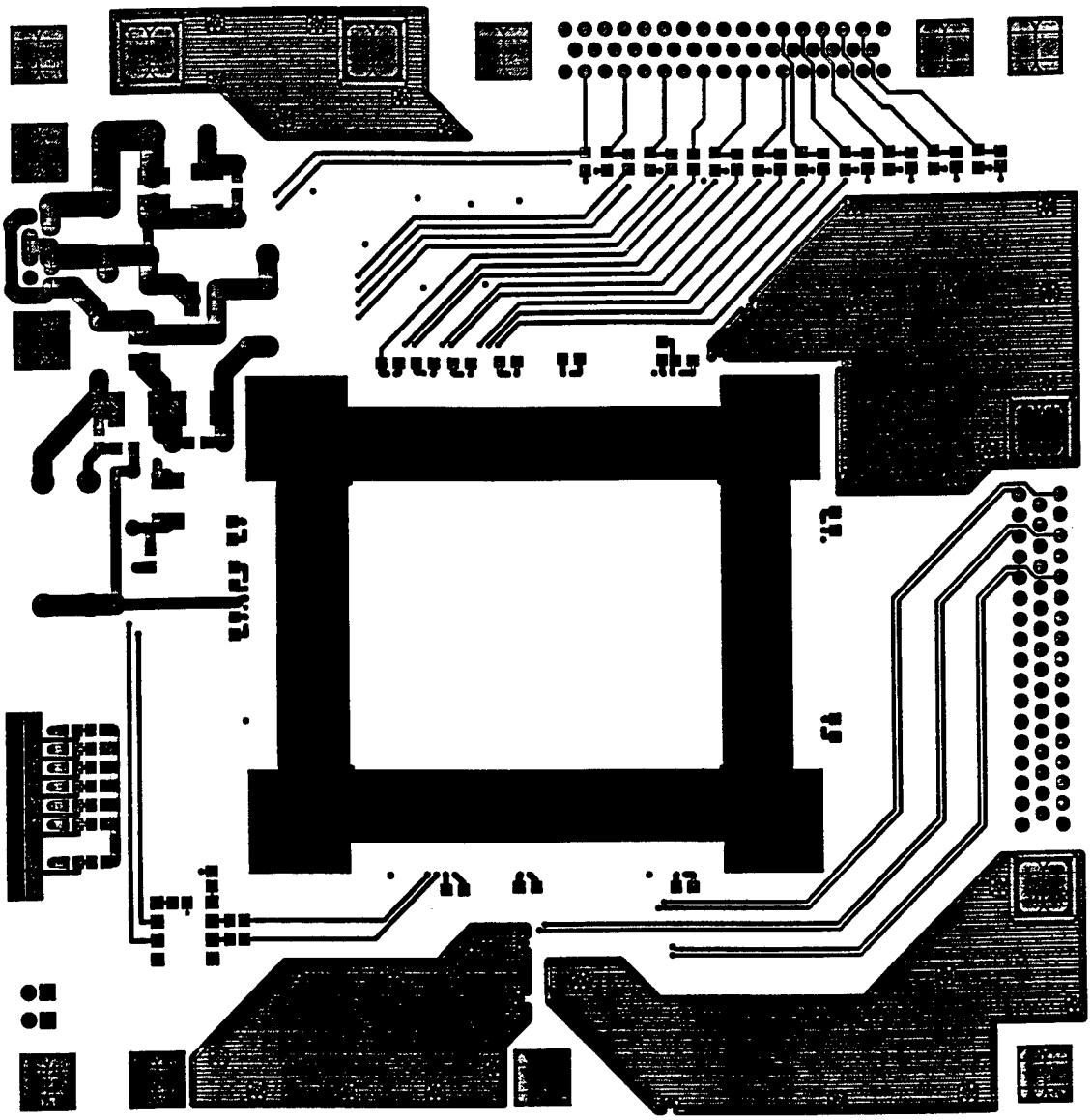
LAYER_3: VCC, VCCA, VCCD (NRL MCM EVAL BRD REV 0.0)



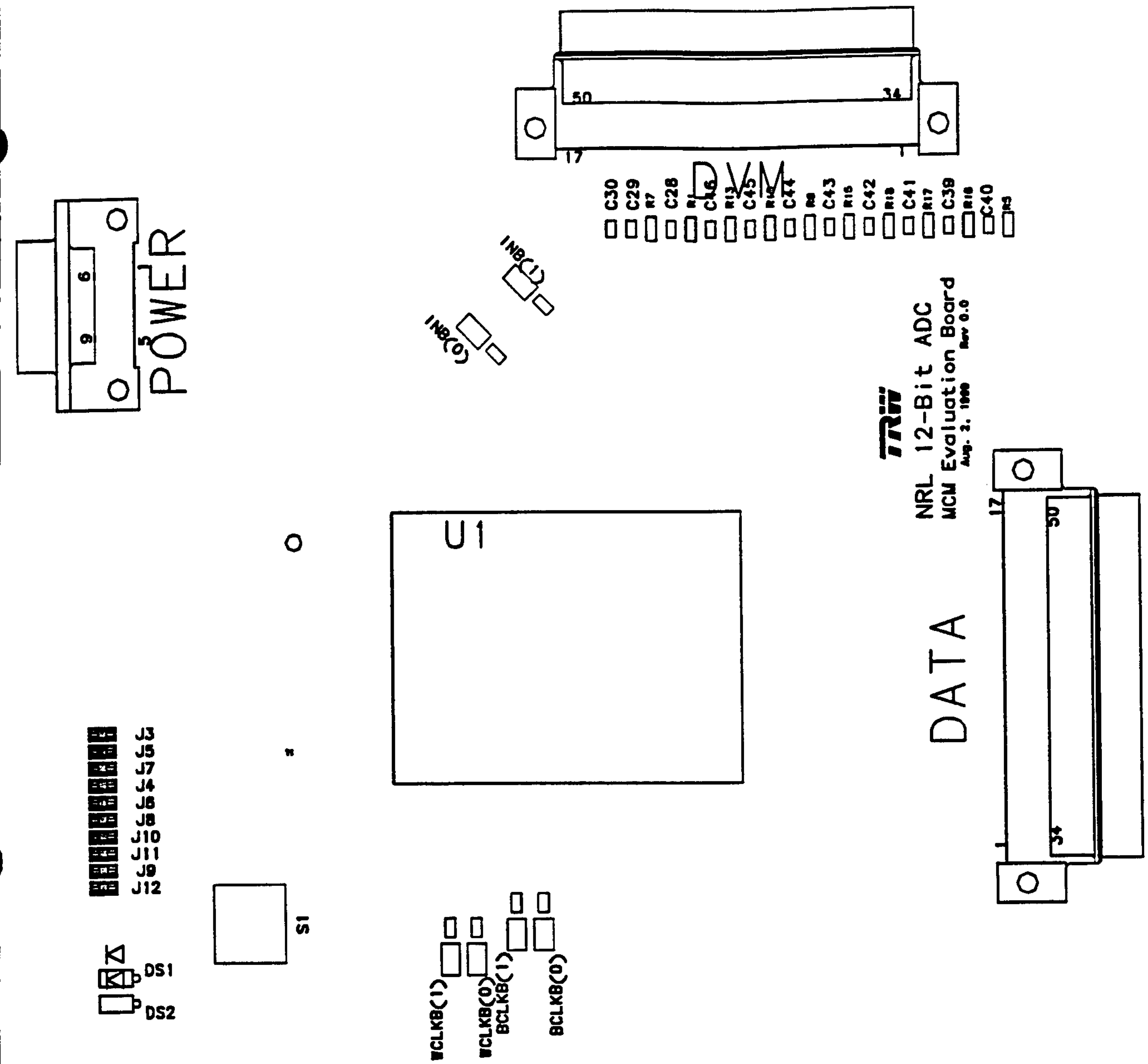
LAYER_4: VEE (NRL MCM EVAL BRD REV 0.0)



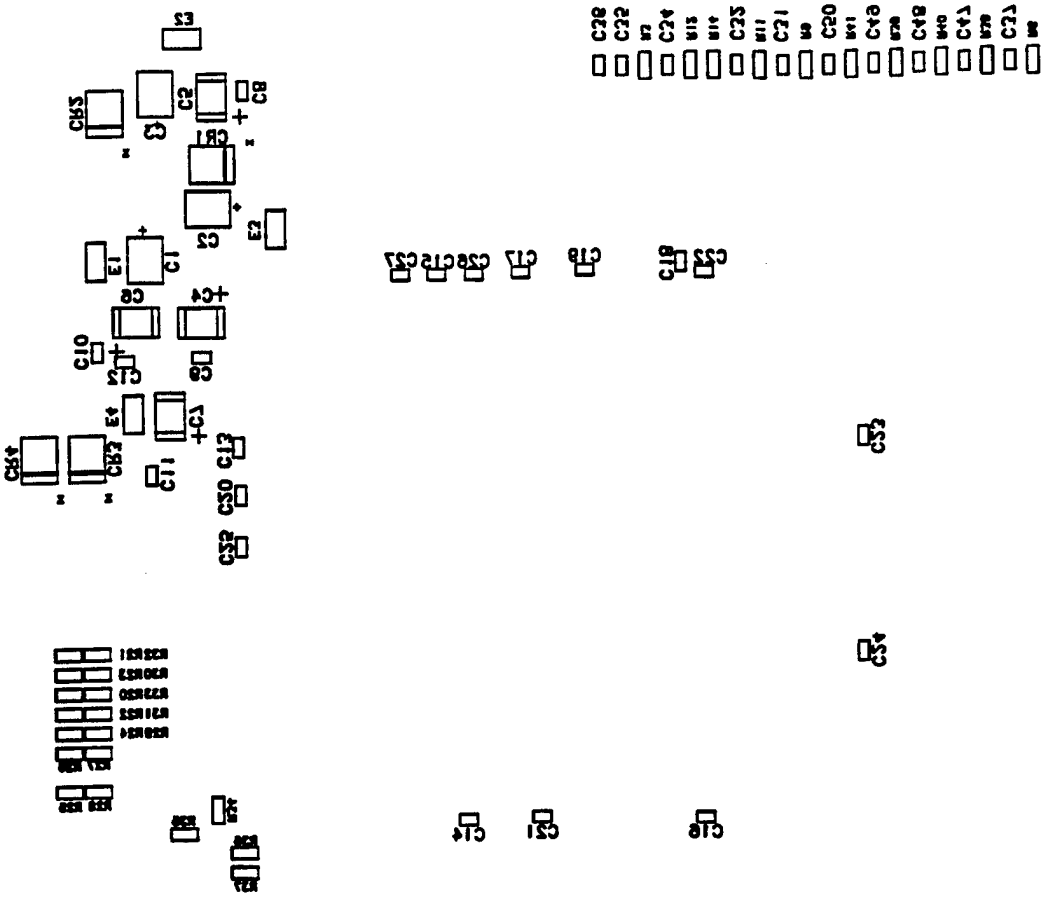
LAYER_5: GROUND (NRL MCM EVAL BRD REV 0.0)



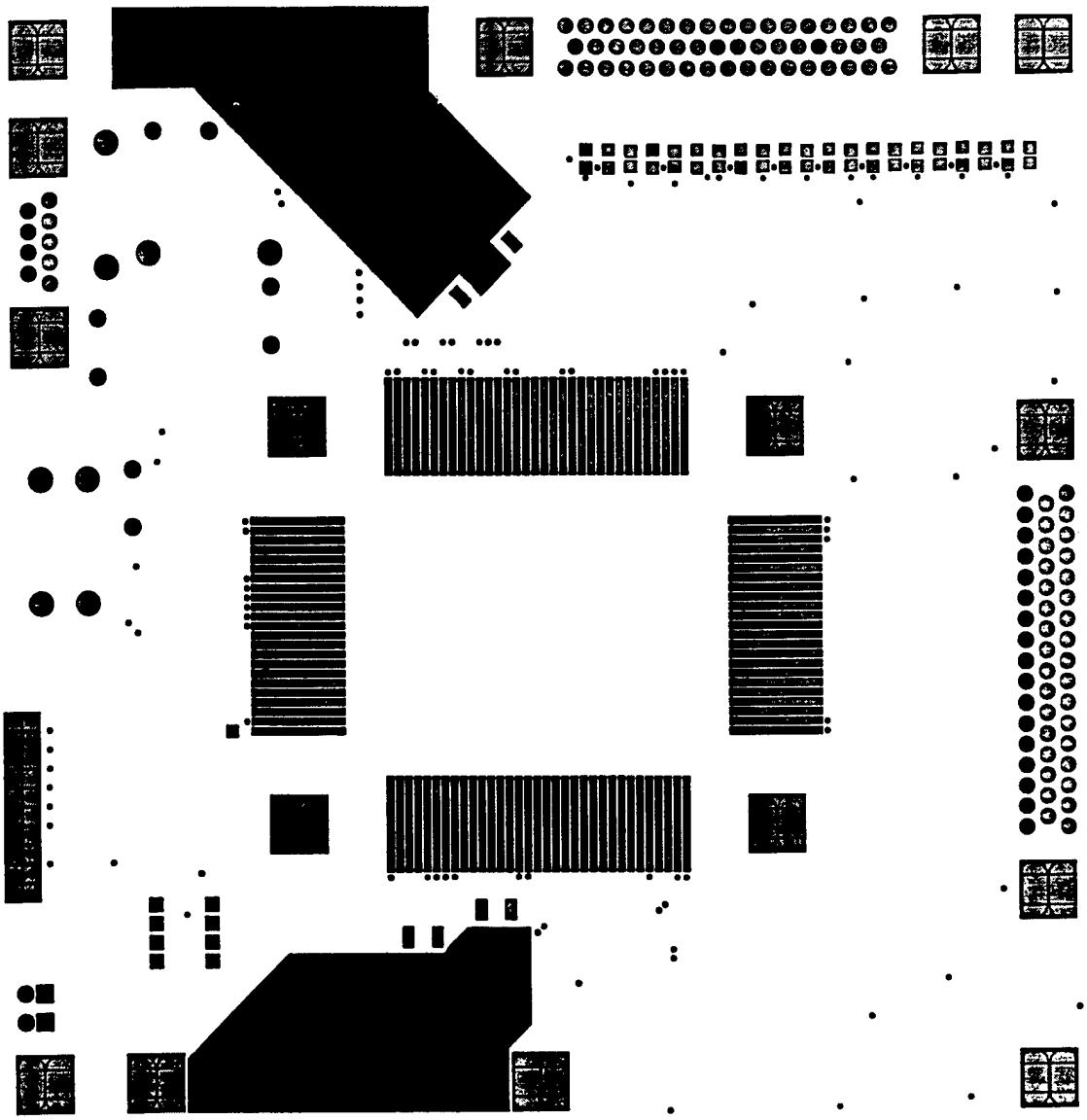
LAYER_6: SIGNAL_2 (NRL MCM EVAL BRD REV 0.0)



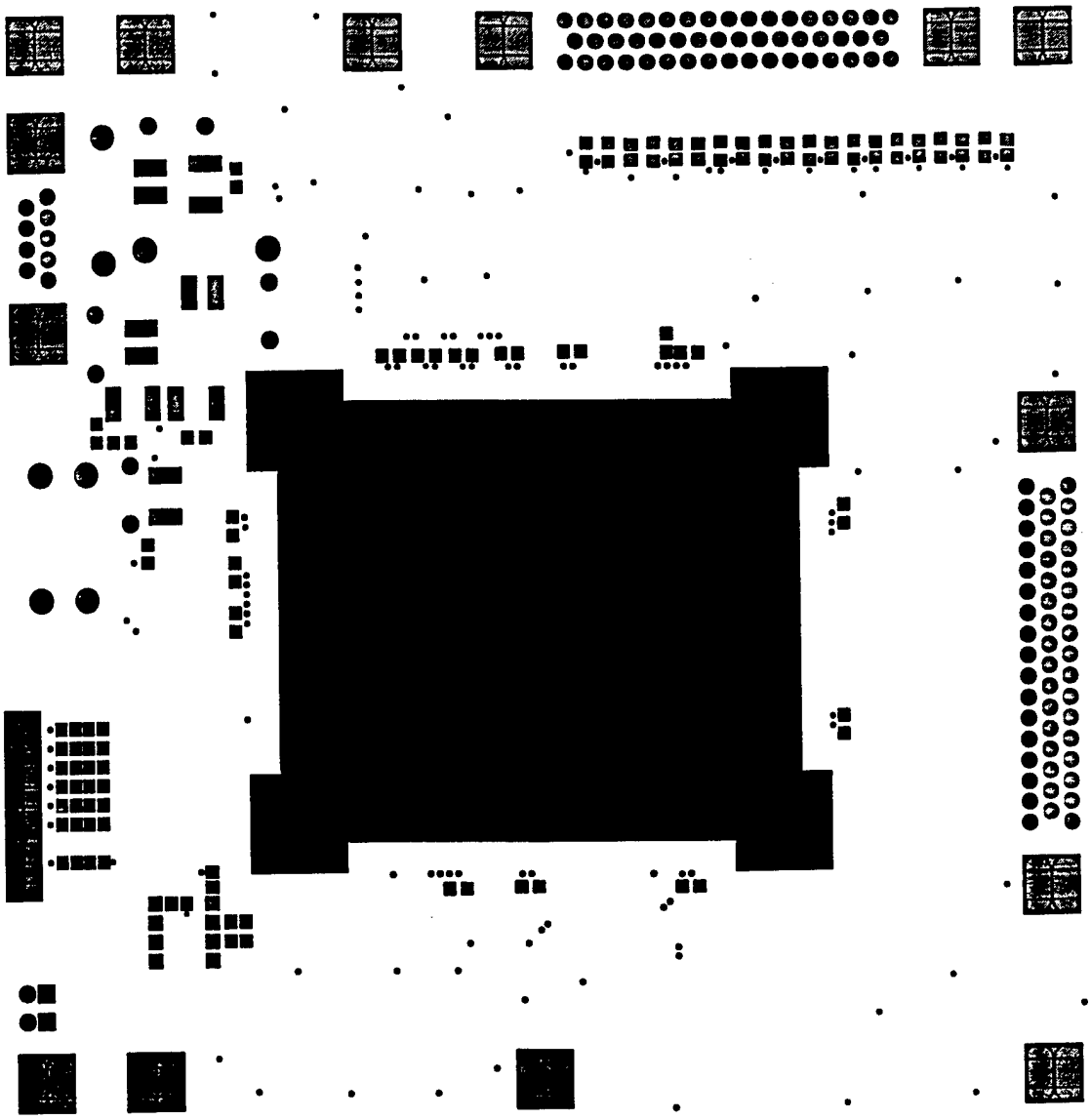
SILKSCREEN_TOP (NRL MCM EVAL BRD REV 0.0)



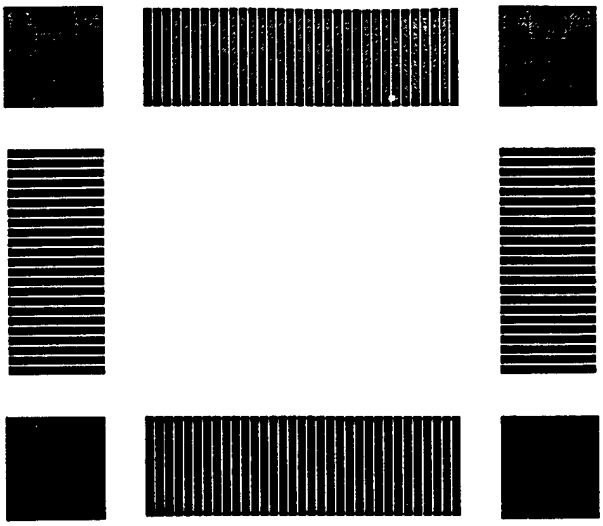
SILKSCREEN_BOTTOM (NRL MCM EVAL BRD REV 0.0)



SOLDER_MASK_TOP (NRL MCM EVAL BRD REV 0.0)



SOLDER_MASK_BOTTOM (NRL MCM EVAL BRD REV 0.0)



GOLD_PLATED_AREA_TOP (NRL MCM EVAL BRD REV 0.0)

GOLD_PLATED_AREA_BOTTOM (NRL MCM EVAL BRD REV 0.0)

TRW Space & Electronics Group

Subject:
Summary of NRL HSAD9 MCM

Date:
August 10, 1999

From:
Khanh Thai
Location/Phone
O2/2374
(310) 813-7995

MCM Summary

• Size L x W x H	2.000" x 1.500" x 0.167"
• No. of leads	112
• Number of Layers	6 Ceramic Layers 7 Metallization Layers
• Power Dissipation	6 Watts
• Technology	HTCC – high temperature cofired ceramic
• Material	Alumina
• Heat Sink	CuW – copper tungsten
• Via Types	0.004 hole w/ 0.008 annular ring 0.008 hole w/ 0.012 annular ring
• Signal Traces	≥ 0.004
• Clearances	≥ design standard in NTK Technical Ceramics Manual

Gerber Format

• Gerber Format:	D-coded assigned, Gerber format
• Aperture Types:	Trace and Flash
• Units:	Inches
• Numeric Format:	6-decimal places

N/C Drill Format

• Drill File Format:	Excellon
• Units:	Inches
• Numeric Format:	Leading / Trailing zero present

Issues and Concerns

- This design is based on the NTK "Special" Design Rules.
  - ➢ It is okay for NTK to adjust Gerber data so that design integrity is consistent with its manufacturing process design rules.
  - ➢ ***TRW must be informed, and approve any design changes to the MCM layout.***
- Expected date of delivery of MCM: September 15, 1999.

Contents of Data Disk

Directory:

/net/cabo/proj61/mgc_d502_chips/AMAD19_1/mcm/amad19_mcm/pcb/mfg/..

Artwork Files:

Gerber Data ***Filename***	Description
TRW_HSAD9.BRZ	Layer 1: Seal Ring Braze Layer Pattern
TRW_HSAD9.SG1	Layer 2: Signal 1 (Top) Pattern
TRW_HSAD9.GD1	Layer 3: Ground 1 Pattern
TRW_HSAD9.VEE	Layer 4: Power VEE Pattern
TRW_HSAD9.VCC	Layer 5: Power VCC, VCCA, VCCD Pattern
TRW_HSAD9.SG2	Layer 6: Signal 2 Pattern
TRW_HSAD9.GD2	Layer 7: Ground 2 Pattern
TRW_HSAD9.SSN	MCM Identification Info for Layer 2

Aperture File:

ASCII Data ***Filename***	Description
TRW_HSAD9_REV.APR	Aperture definitions (revised)

Drill Data Files:

Excellon Data ***Filename***	Description
thr_BRZG2	Through Via from Braze (layer 1) to Ground 2 (layer 7)
bv_BRZS1	Buried Via from Braze (layer 1) to Signal 1 (layer 2)
bv_S1G1	Buried Via from Signal 1 (layer 2) to Ground 1 (layer 3)
bv_S1VEE	Buried Via from Signal 1 (layer 2) to VEE (layer 4)
bv_S1VCC	Buried Via from Signal 1 (layer 2) to VCC (layer 5)
bv_S1S2	Buried Via from Signal 1 (layer 2) to Signal 2 (layer 6)
bv_G1G2	Buried Via from Ground 1 (layer 3) to Ground 2 (layer 7)

Attachments:

- **Aperture Table:**
  A list of different aperture types used in the layout.

- **Via Definitions:**
  Shows the different types and sizes of vias used. Includes the via naming conventions.

- **Mechanical Drawings:**
  112 Lead HTCC MCM Package
  MCM Layers (side view)
  MCM Cover

- **Power and Signal Layers Drawings:**
  Hard copies of the Artwork files created in Mentor Graphics MCM station.
  Layer 1: Seal Ring Braze Layer Pattern
  Layer 2: Signal 1 (Top) Pattern
  Layer 3: Ground 1 Pattern
  Layer 4: Power VEE Pattern
  Layer 5: Power VCC, VCCA, VCCD Pattern
  Layer 6: Signal 2 Pattern
  Layer 7: Ground 2 Pattern
  MCM Identification Info for Layer 2

- **MCM Schematics:**
  amad19_mcm (Mentor Graphics)

- **MCM Station BOM (Bill Of Materials) file:**
  This file lists all the parts used in the MCM. These components are stored in the cell library in Mentor Graphics MCM Station: **/net/cabo/proj61/ mgc_d502_chips/AMAD19_1/mcm/amad19_mcm/design_geom/..**

- **Wire Bonding Diagrams:**
  All wire bonds are 1 mil gold wire (C600218-2)
  There are approximately 410 bonding wires.

APERTURE TABLE:

Tuesday July 13, 1999; 11:45:22

Position	Shape	Type	Width(X)	Height(Y)/Diameter	Orientation	Mirror	Power	Dcode	Used Last Run
1	circle	trace	0.000000	0.004000	0	false	false	10	false
2	circle	trace	0.000000	0.012000	0	false	false	11	false
3	circle	trace	0.000000	0.010000	0	false	false	12	false
4	circle	trace	0.000000	0.025000	0	false	false	13	false
5	circle	trace	0.000000	0.008000	0	false	false	14	false
6	circle	trace	0.000000	0.005000	0	false	false	15	false
7	circle	trace	0.000000	0.006000	0	false	false	16	false
8	rectangle	flash	0.050000	0.035000	0	false	false	17	false
9	rectangle	flash	0.035000	0.050000	0	false	false	18	false
10	rectangle	flash	0.050000	0.025000	0	false	false	19	false
11	rectangle	flash	0.060000	0.035000	0	false	false	70	false
12	rectangle	flash	0.068000	0.068000	0	false	false	71	false
13	rectangle	flash	0.025000	0.030000	0	false	false	20	false
14	rectangle	flash	0.004000	0.004000	0	false	false	21	false
15	rectangle	flash	0.005000	0.005000	0	false	false	22	false
16	rectangle	flash	0.006000	0.006000	0	false	false	23	false
17	rectangle	flash	0.030000	0.025000	0	false	false	24	false
18	rectangle	flash	0.010000	0.010000	0	false	false	25	false
19	rectangle	flash	0.030000	0.035000	0	false	false	26	false
20	rectangle	flash	0.025000	0.050000	0	false	false	27	false
21	rectangle	flash	0.035000	0.030000	0	false	false	28	false
22	rectangle	flash	0.006000	0.012000	0	false	false	29	false
23	circle	trace	0.000000	0.001000	0	false	false	72	false
24	circle	trace	0.000000	0.002000	0	false	false	73	false
25	circle	flash	0.000000	0.012000	0	false	false	125	false
26	circle	flash	0.000000	0.008000	0	false	false	126	false

Object Painting

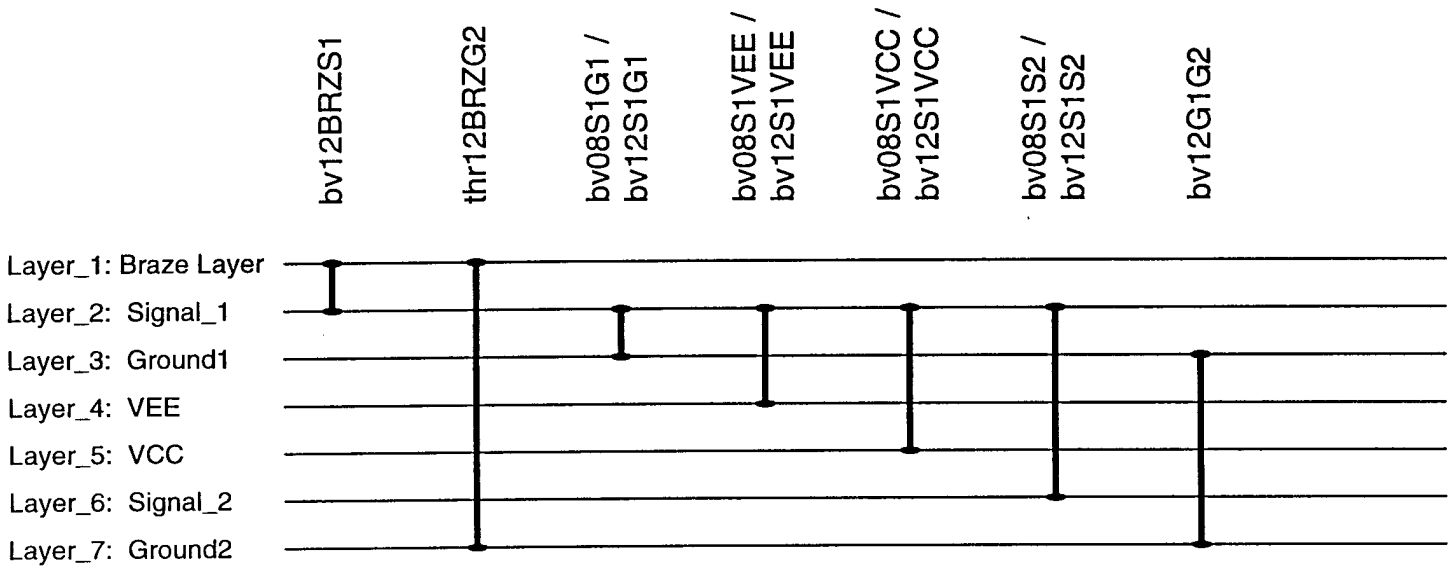
Aperture Position	Resolution
23	0.000800

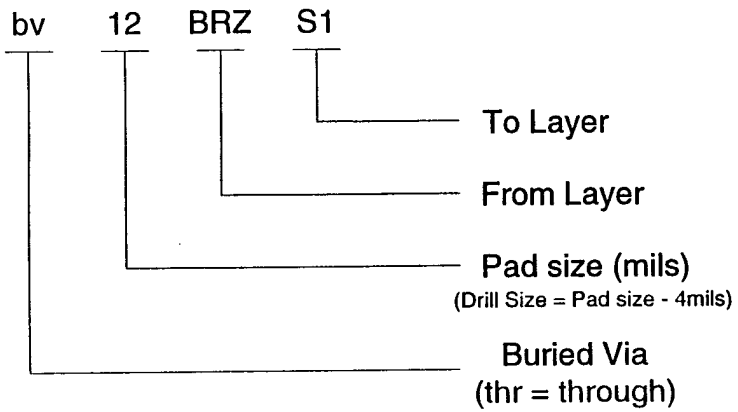
Area Fill Aperture

Aperture Position	Spacing	
23	0.004000	0.004000

Thermal tie aperture 23

Via Definitions:

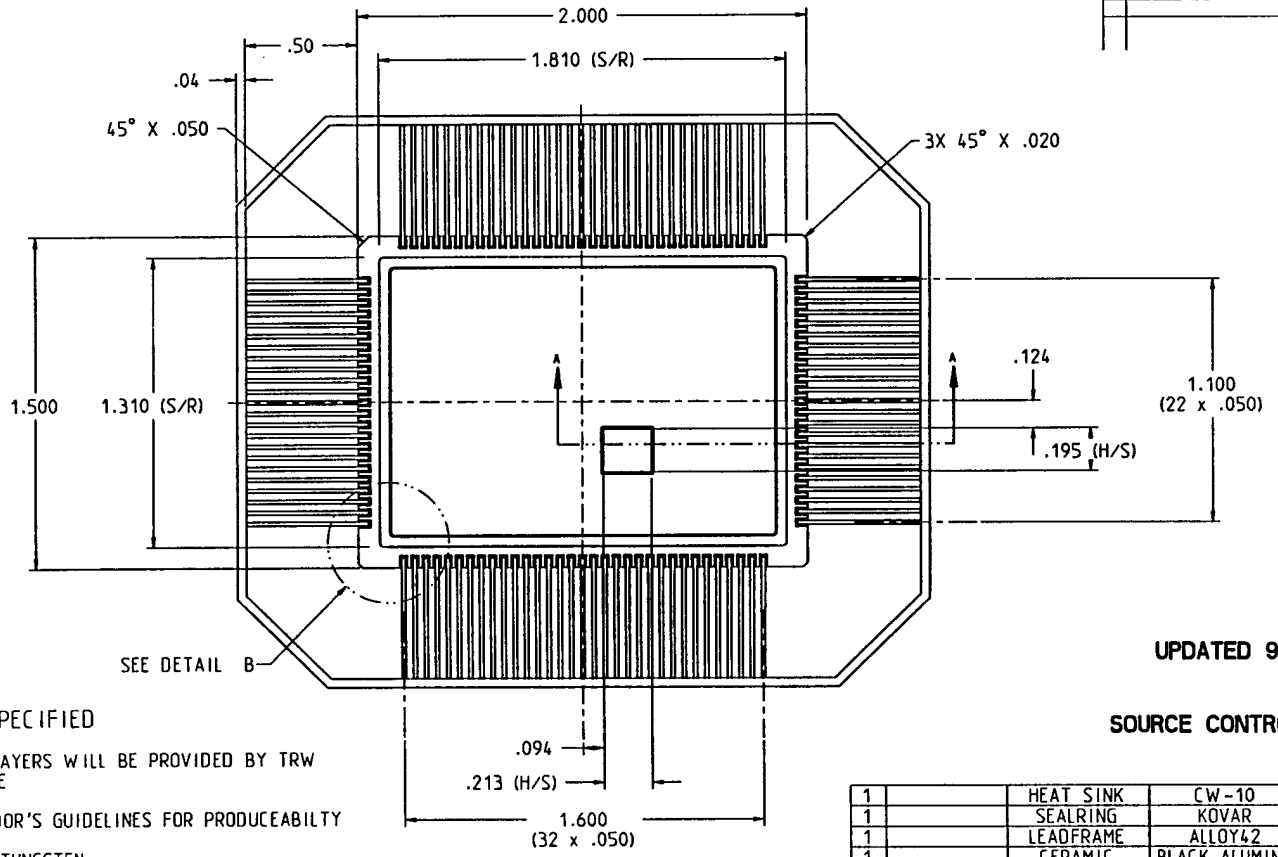




BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.004	205	YES	---
⊞	.008	277	YES	---

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



UPDATED 99-06-28

SOURCE CONTROL DRAWING

NOTES: UNLESS OTHERWISE SPECIFIED

1. METALIZATION PATTERN FOR ALL LAYERS WILL BE PROVIDED BY TRW VIA GERBER ELECTRONIC DATABASE
2. DESIGN WILL BE DONE WITH VENDOR'S GUIDELINES FOR PRODUCEABILTY
3. METALIZATION TO BE THICK FILM TUNGSTEN.
4. SEALRING AND HEATSINK TO BE ELECTRICALLY CONNECTED TO THE GROUND PLANE.
5. ELECTROPLATE LEADS, SEALRING, AND EXPOSED METALIZATION WITH NICKEL PER MIL-M-38510, 50-350 MICROINCHES, PER QQ-N-290. NICKEL PLATING SHALL BE FOLLOWD BY GOLD PLATING PER MIL-G-45204, TYPE III, CLASS 2, 100 MICROINCHES MINIMUM
6. LEADFRAME HAS 112 PINS [(23 + 33) x 2]
7. TRW SPEC #D01902 SHALL APPLY
8. ALL .XXX DIMENSIONS ARE ±.005

PARTS LIST

ITEM NO.	ZONE	REF. DES.	SPEC.	MATERIAL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.		
4				CW-10	HEAT SINK			1
3			ASTM F-15	KOVAR	SEALRING			1
2				ALLOY42	LEADFRAME			1
1				BLACK ALUMINA	CERAMIC			1

UNLESS OTHERWISE SPECIFIED
1. DO NOT SCALE DRAWING.
2. INTERPRET PER DOD-STD-100.
3. DIMENSIONS ARE IN INCHES. NA
4. SURFACE TEXTURE SHALL BE
5. REMOVE BURRS AND SHARP EDGES.
6. DIMENSIONS APPLY BEFORE PLATING OR CONVERSION COATING.
7. PARENTHETICAL DATA IS FOR REFERENCE ONLY

TOLERANCES ON ALL HOLE DIAMETERS

UNDER .0140	+.0020 -.0005	.501 THRU .750	+.008 -.001
.014 THRU .125	+.004 -.003	.751 THRU 1.000	+.010 -.001
.126 THRU .250	+.005 -.001	1.000 THRU 1.999	+.012 -.001
.251 THRU .500	+.006 -.001		

TOLERANCE ON DECIMAL DIMENSIONS: .XXX ±.010, .XX ±.03, .X ±.1

TOLERANCE ON ANGULAR DIMENSIONS: MACHINED ±0°30', LOCATING ±0°30', ASSMYD ±1°, CHAMFERS ±5°

APPLICABLE SPECIFICATIONS: THE ABOVE TRW SREG SPECS FORM A PART OF THIS DRAWING

FINISH

HEAT TREAT

CONTRACT NO.		
ISSUED	S VANLIEW	99-05-3
CHECKED		
ENGINEER		
RDE		
MFG		
M&P		
STRESS		
THERMAL		

THE FOLLOWING ECO'S HAVE BEEN ATTACHED TO THIS PRINT

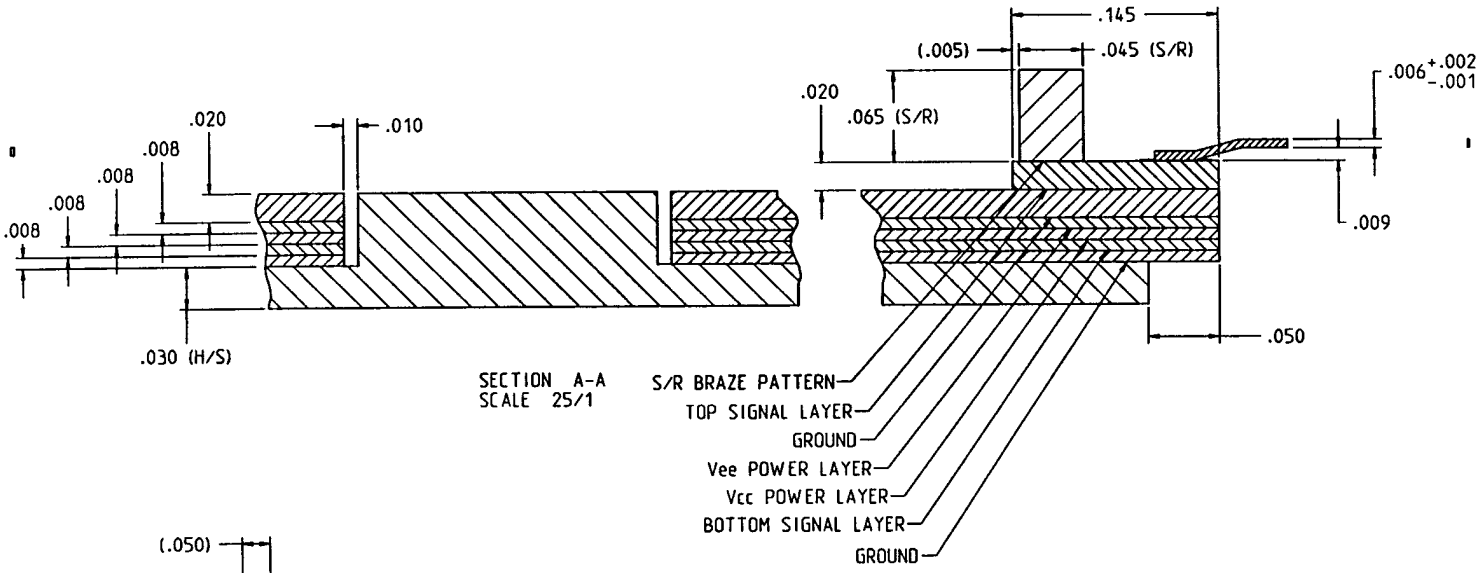
TRW Space & Electronics Group
One Space Park
Redondo Beach, CA 90278

112 LEAD HTCC MCM PACKAGE

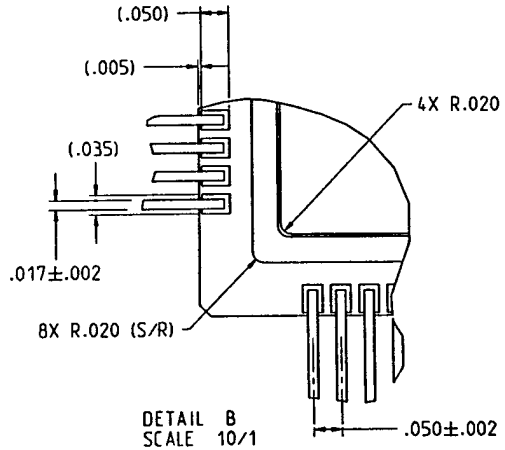
USED ON APPLICATION	CI NO.	NEXT ASSY	NEXT ASSY QTY REQD	FINAL ASSY QTY REQD

SIZE	CAGE CODE		REV
D	11982	TRW_HSAD9	-
SCALE		SHEET 1 OF 2	

Pro/E



SECTION A-A
SCALE 25/1

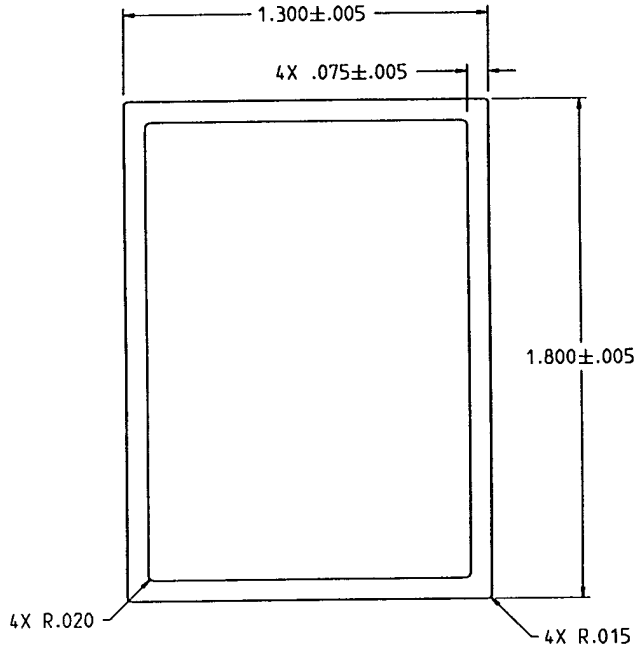


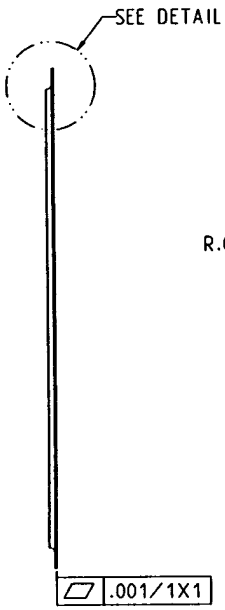
DETAIL B
SCALE 10/1

SIZE	CAGE CODE		REV
D	11982	TRW_HSAD9	-
SCALE		SHEET	

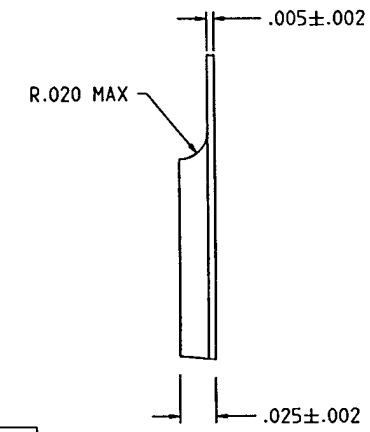
Pro/E

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





DETAIL A
SCALE 25/1



NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: KOVAR SHEET (ASTM F-15), ANNEALED, PER MIL-I-23001, CLASS 1

2. ELECTROPLATE NICKEL PER MIL-M-38510. NICKEL THICKNESS MUST BE BETWEEN 50 - 350 MICROINCHES, PER QQ-N-290. NICKEL PLATING SHALL BE FOLLOWED BY GOLD PER MIL-G-45204, TYPE III, CLASS 2, 100 MICROINCHES MINIMUM.

UNLESS OTHERWISE SPECIFIED
1. DO NOT SCALE DRAWING.
2. INTERPRET PER DOD-STD-100.
3. DIMENSIONS ARE IN INCHES. MA
4. SURFACE TEXTURE SHALL BE
5. REMOVE BURRS AND SHARP EDGES.
6. DIMENSIONS APPLY BEFORE PLATING OR CONVERSION COATING.
7. PARENTHETICAL DATA IS FOR REFERENCE ONLY

TOLERANCES ON ALL HOLE DIAMETERS

UNDER .0110	+.0020 -.0005	.501 THRU .750	+.008 -.001
.01 THRU .125	+.004 -.001	.751 THRU 1.000	+.010 -.001
.126 THRU .250	+.005 -.001	1.000 THRU 1.999	+.012 -.001
.251 THRU .500	+.006 -.001		

TOLERANCE ON DECIMAL DIMENSIONS: .XXX ±.010, .XX ±.03, .X ±.1

TOLERANCE ON ANGULAR DIMENSIONS: MACHINED ±0°30', LOCATING ±0°10', BENDS ±2°, CHAMFERS ±5°

FINISH

HEAT TREAT

APPLICABLE SPECIFICATIONS
THE ABOVE TRW SCITC SPECS FORM A PART OF THIS DRAWING

USED ON | CI NO. | NEXT ASSY
APPLICATION

NEXT ASSY BIT MOD | FINAL ASSY BIT MOD

CONTRACT NO.	&Contract No	
DRAWN S. VANLIEW	99-06-28	
CHECKED &Checked By	&Date_Chk	
ENGINEER &Engineer	&Date_Eng	
RDE &RDE	&Date_RDE	
MFG &Mfg Engineer	&Date_Mfg	
MP &M.&P Engineer	&Date_MP	
STRESS &Stress Engineer	&Date_Anal	
THERMAL &Thermal Engineer	&Date_Ther	

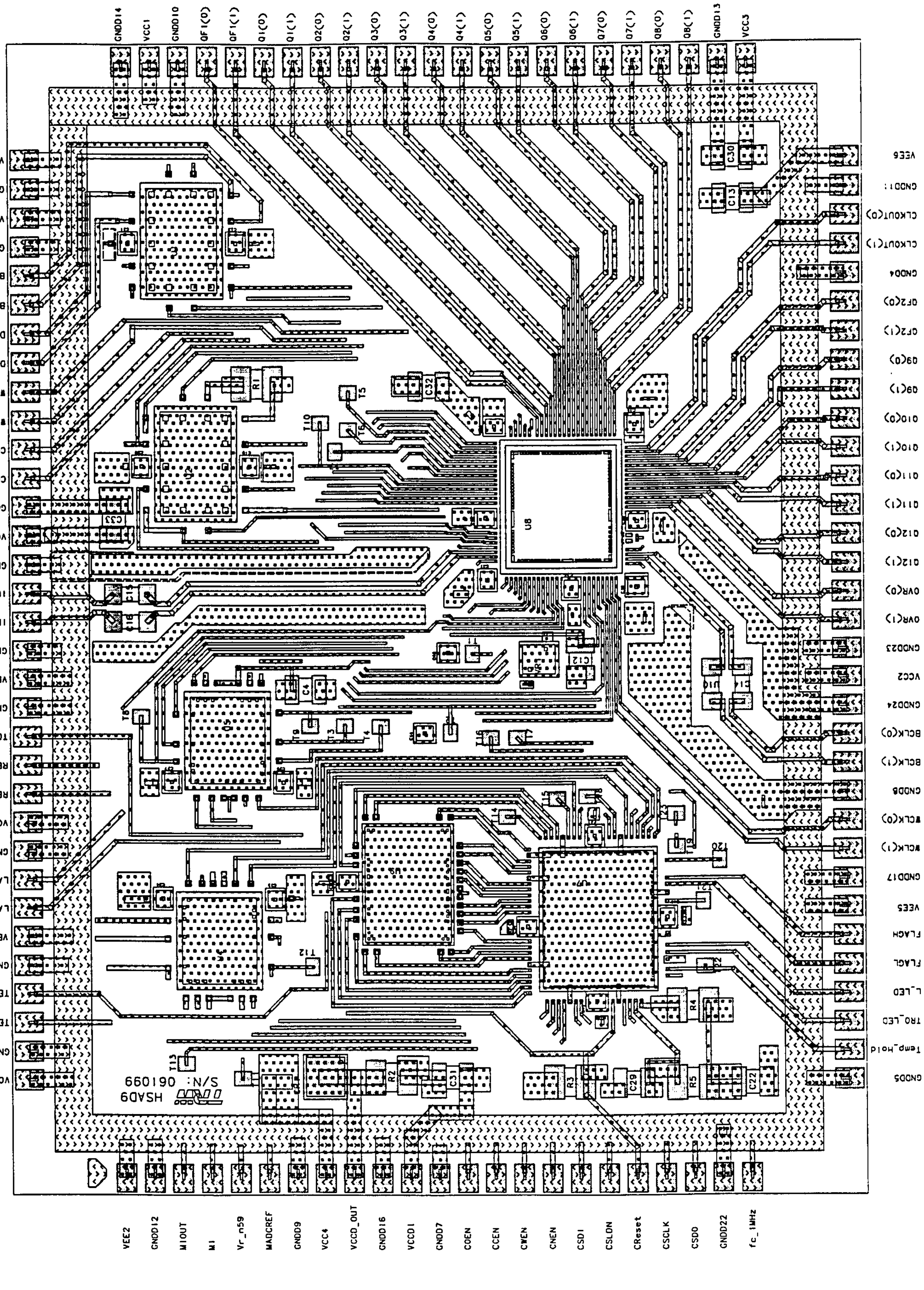
THE FOLLOWING EO'S HAVE BEEN ATTACHED TO THIS PRINT

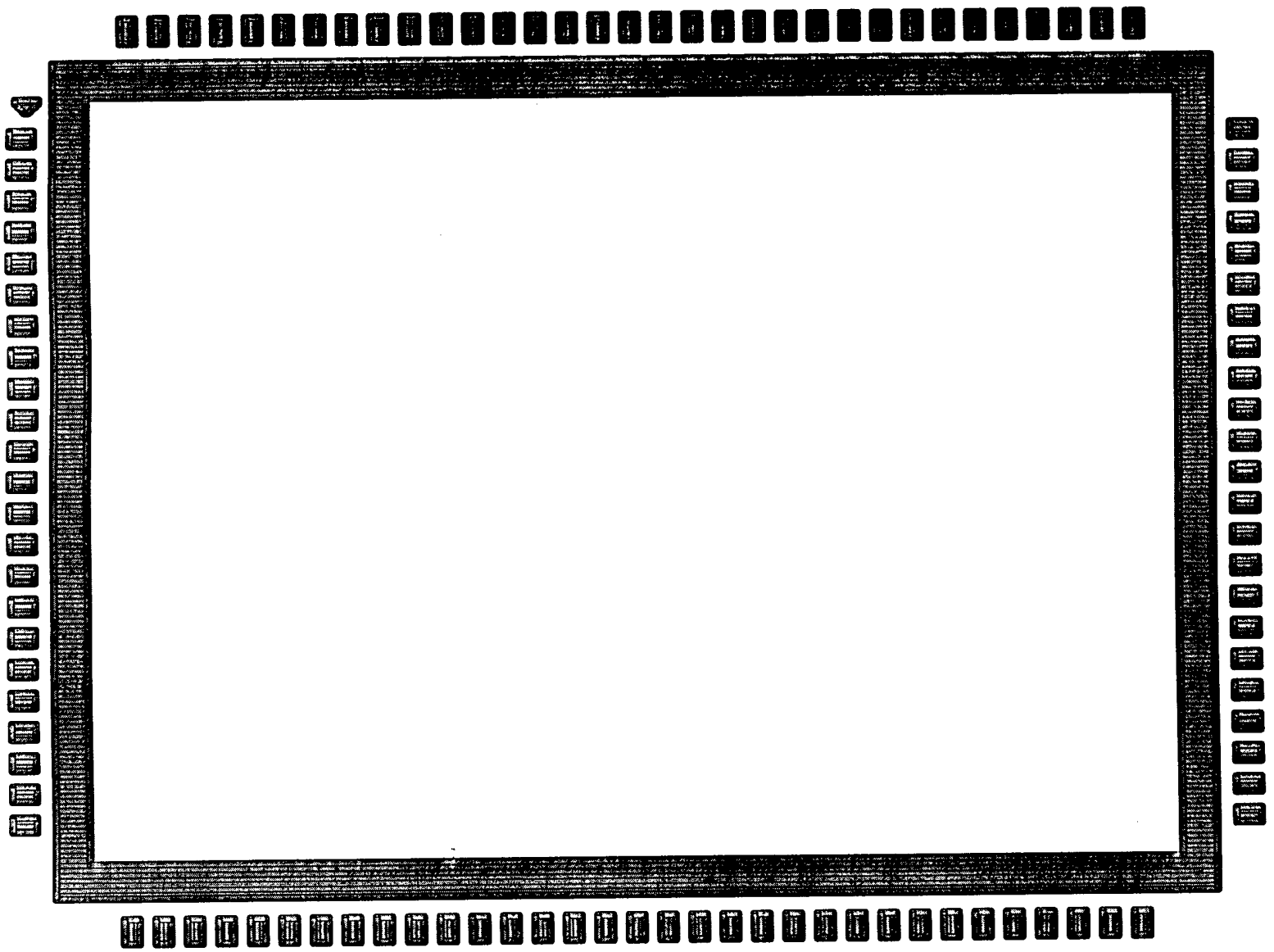
TRW Space & Electronics Group
One Space Park
Redondo Beach, CA 90278

COVER, HSAD9 MCM

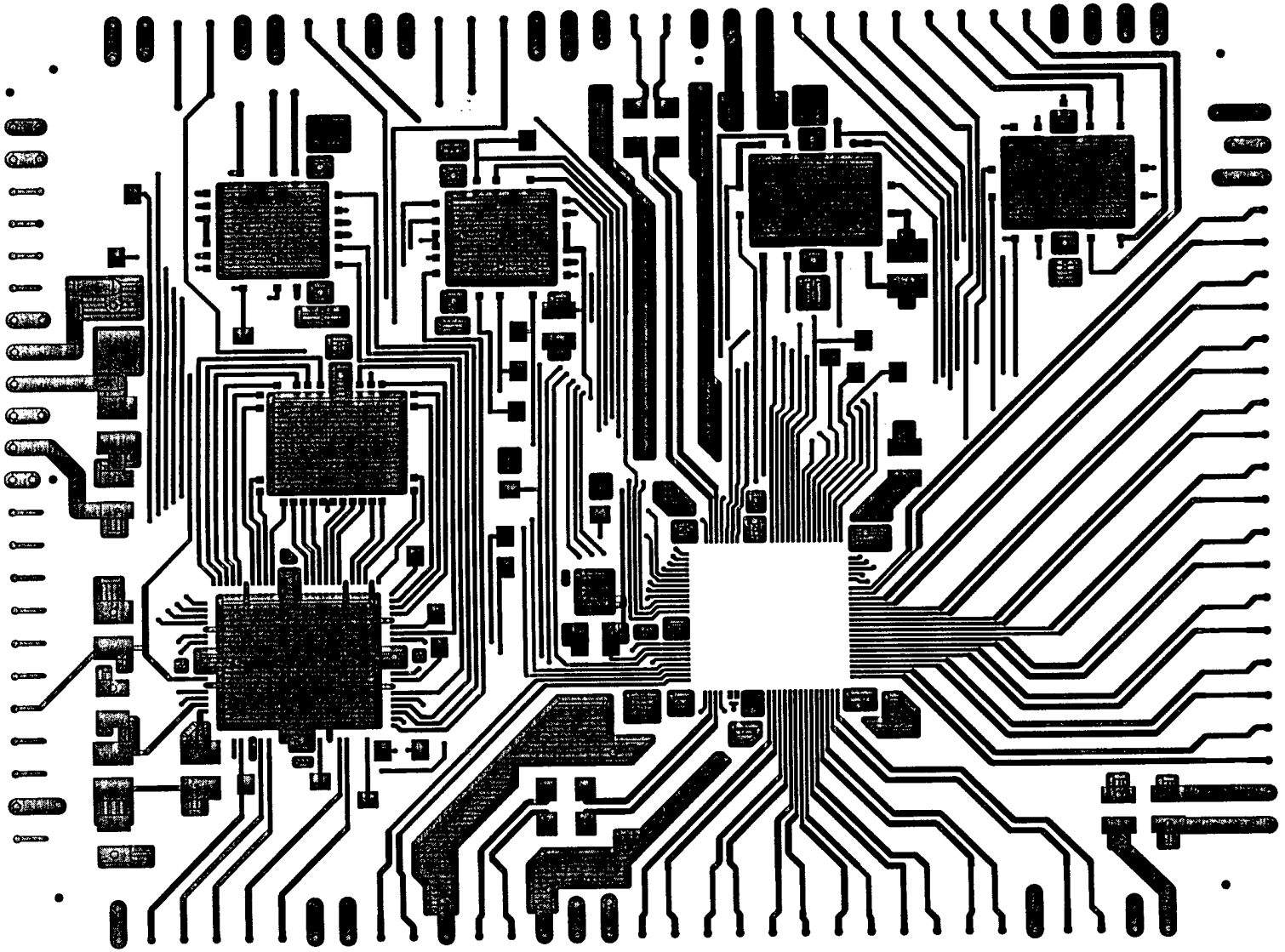
SIZE	CAGE CODE		REV
D	11982	HSAD9_LID	-
SCALE		SHEET 1 OF 1	

Pro/E

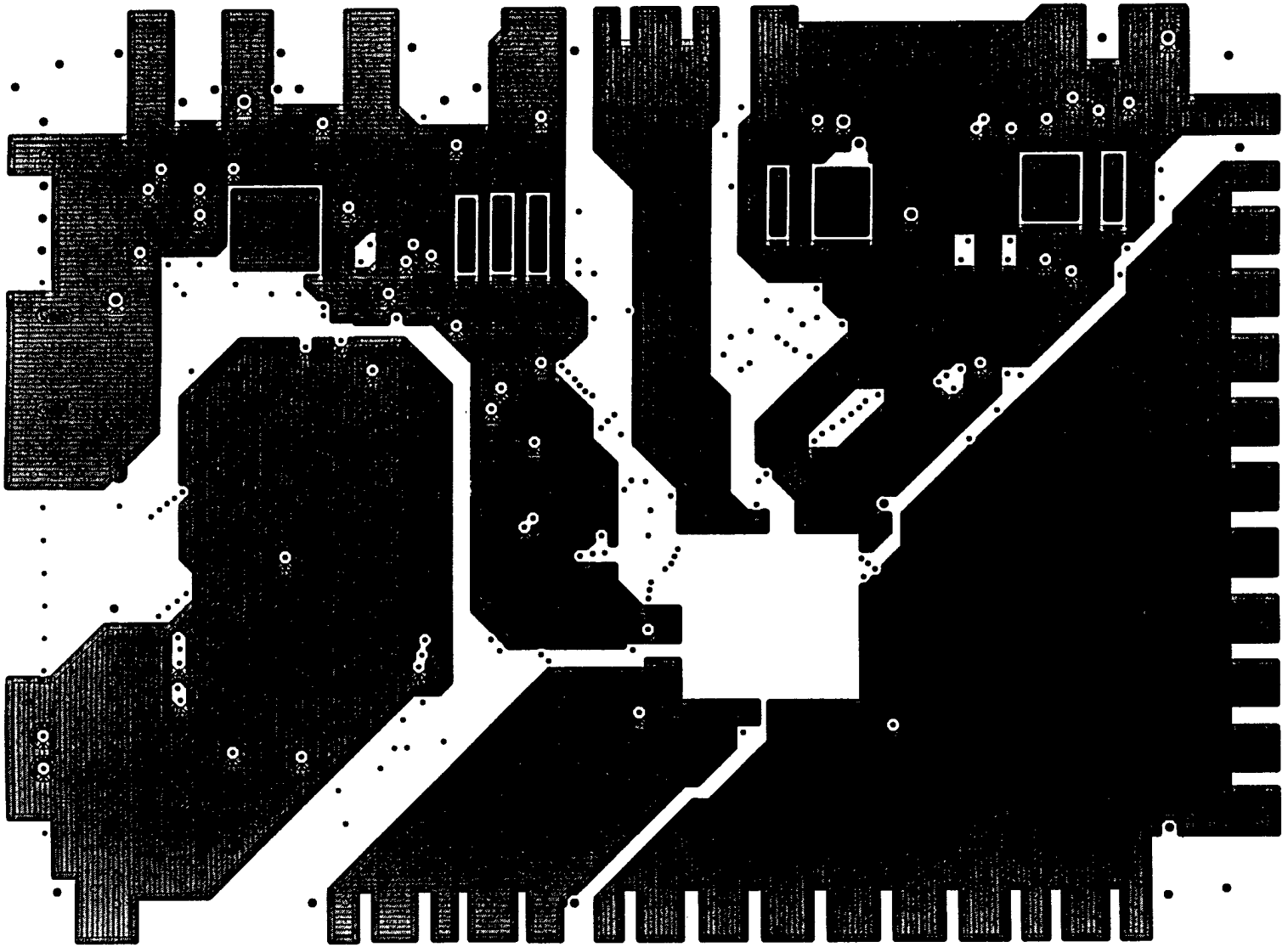

GNDD14
VCC1
GNDD10
QF1(0)
QF1(1)
Q1(0)
Q1(1)
Q2(0)
Q2(1)
Q3(0)
Q3(1)
Q4(0)
Q4(1)
Q5(0)
Q5(1)
Q6(0)
Q6(1)
Q7(0)
Q7(1)
Q8(0)
Q8(1)
GNDD13
VCC3
VEE2
GNDD12
MIOUT
MI
Vr_n59
MADCREF
GNDD9
VCC4
VCCD_OUT
GNDD16
VCCD1
GNDD7
COEN
CCEN
CWEN
CNEN
CSDI
CSLON
CReset
CSCLK
CSDO
GNDD22
fc_1MHz
HSAD9
S/N 061099



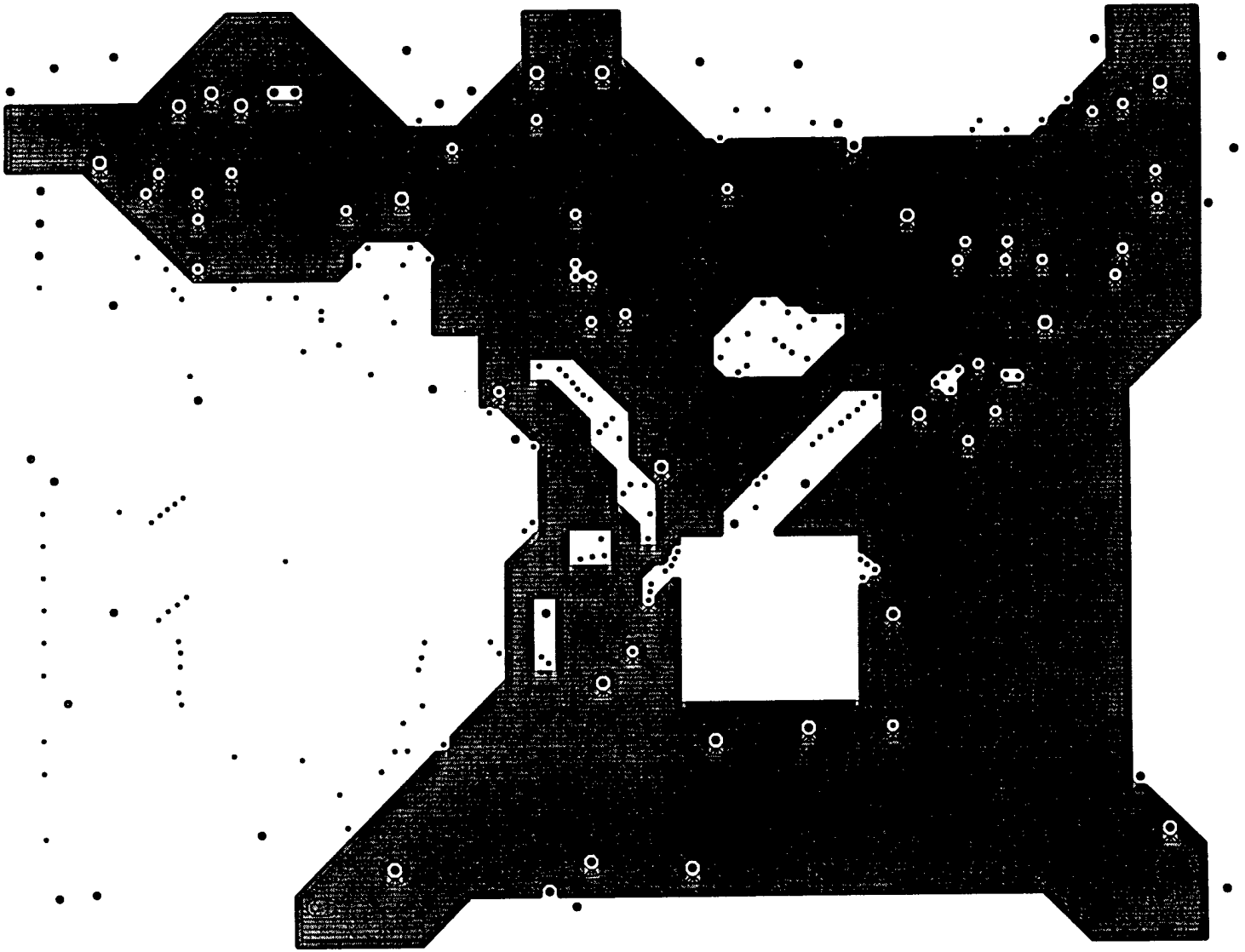
LAYER_1: BRAZE_LAYER (HSAD9 MCM)



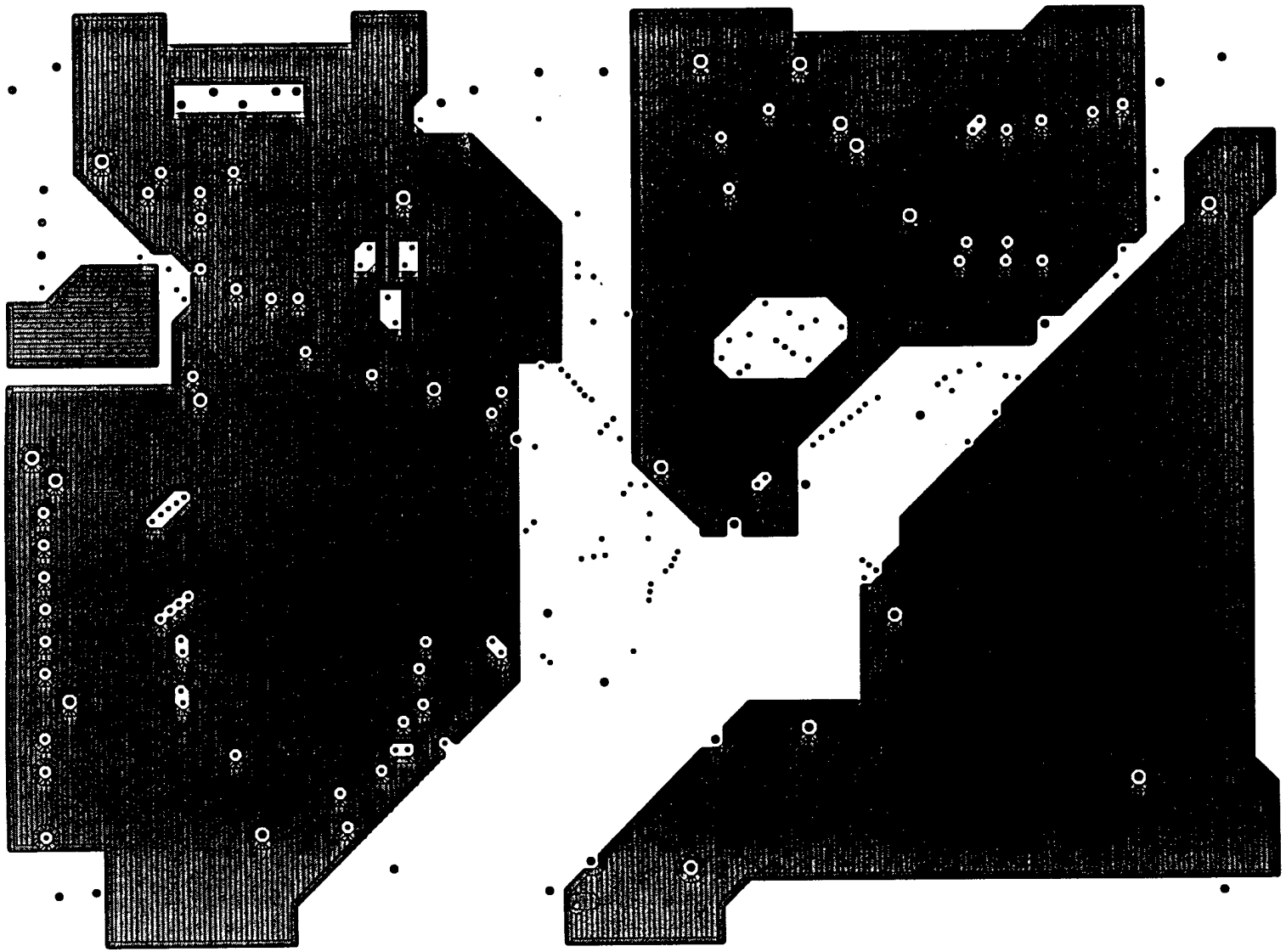
LAYER_2: SIGNAL_1 (HSAD9 MCM)



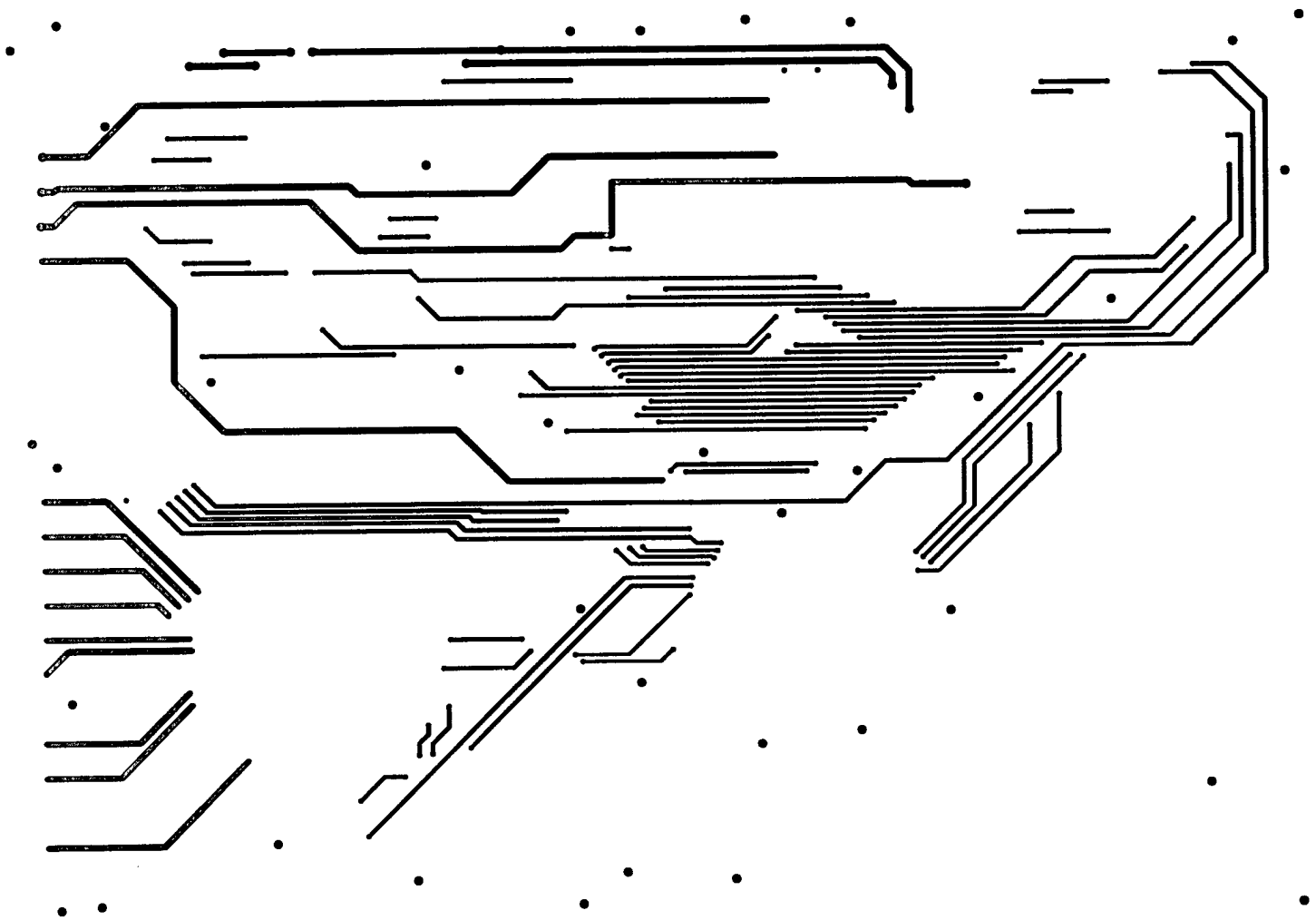
LAYER_3: GROUND1 (HSAD9 MCM)



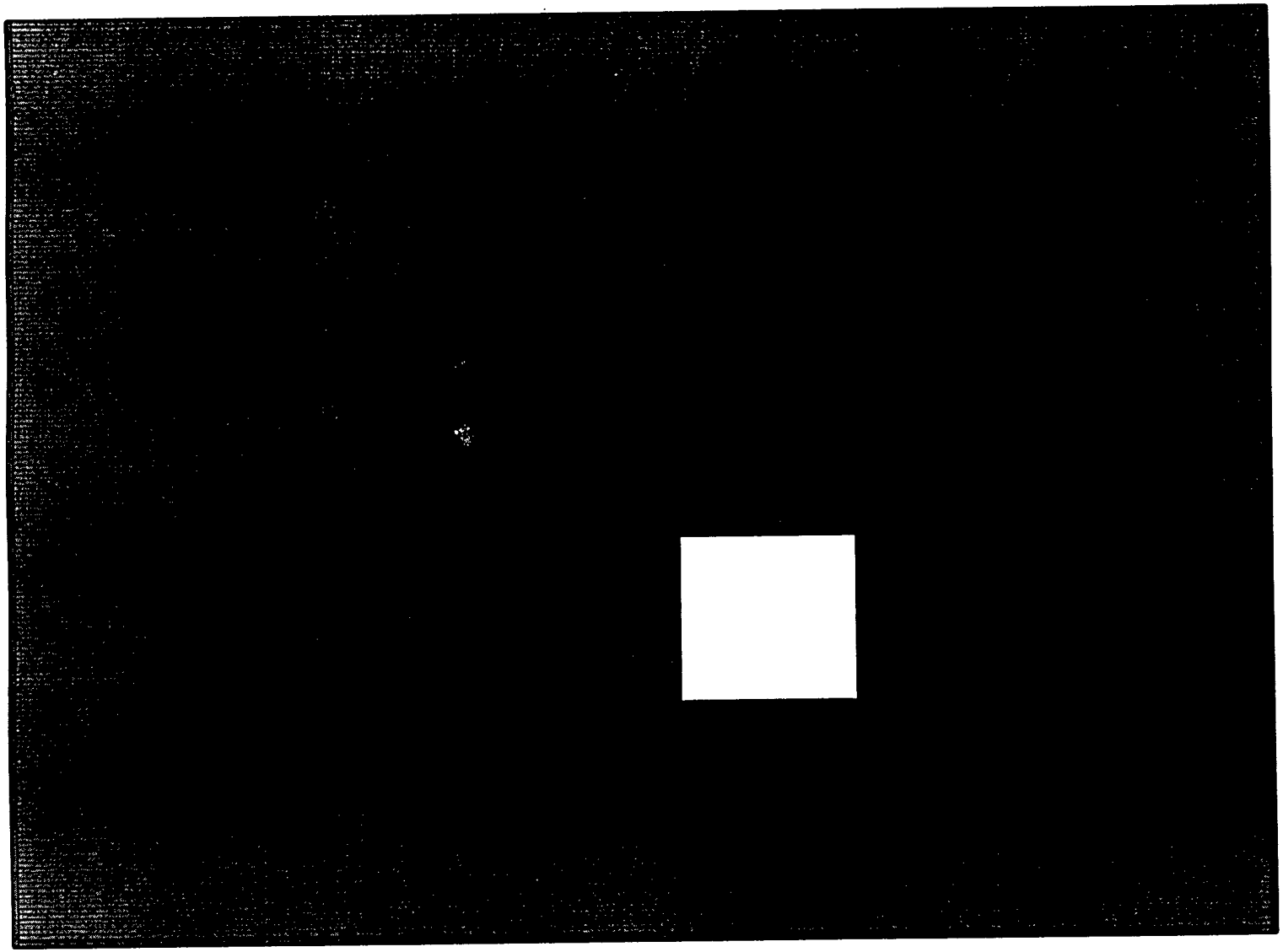
LAYER_4: VEE (HSAD9 MCM)



LAYER_5: VCC (HSAD9 MCM)



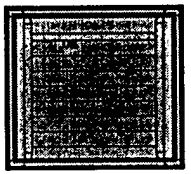
LAYER_6: SIGNAL_2 (HSAD9 MCM)



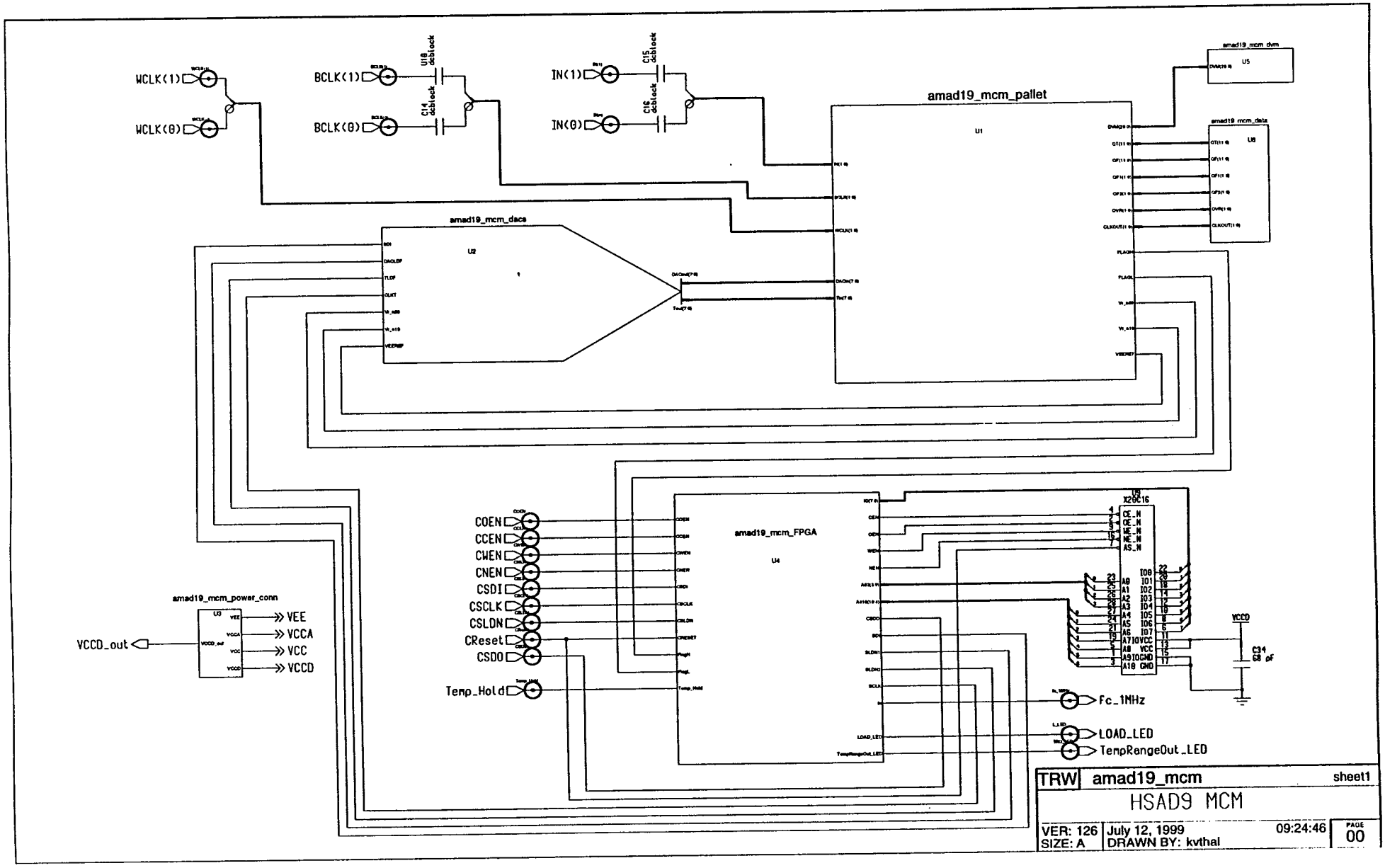
LAYER_7: GROUND2 (HSAD9 MCM)

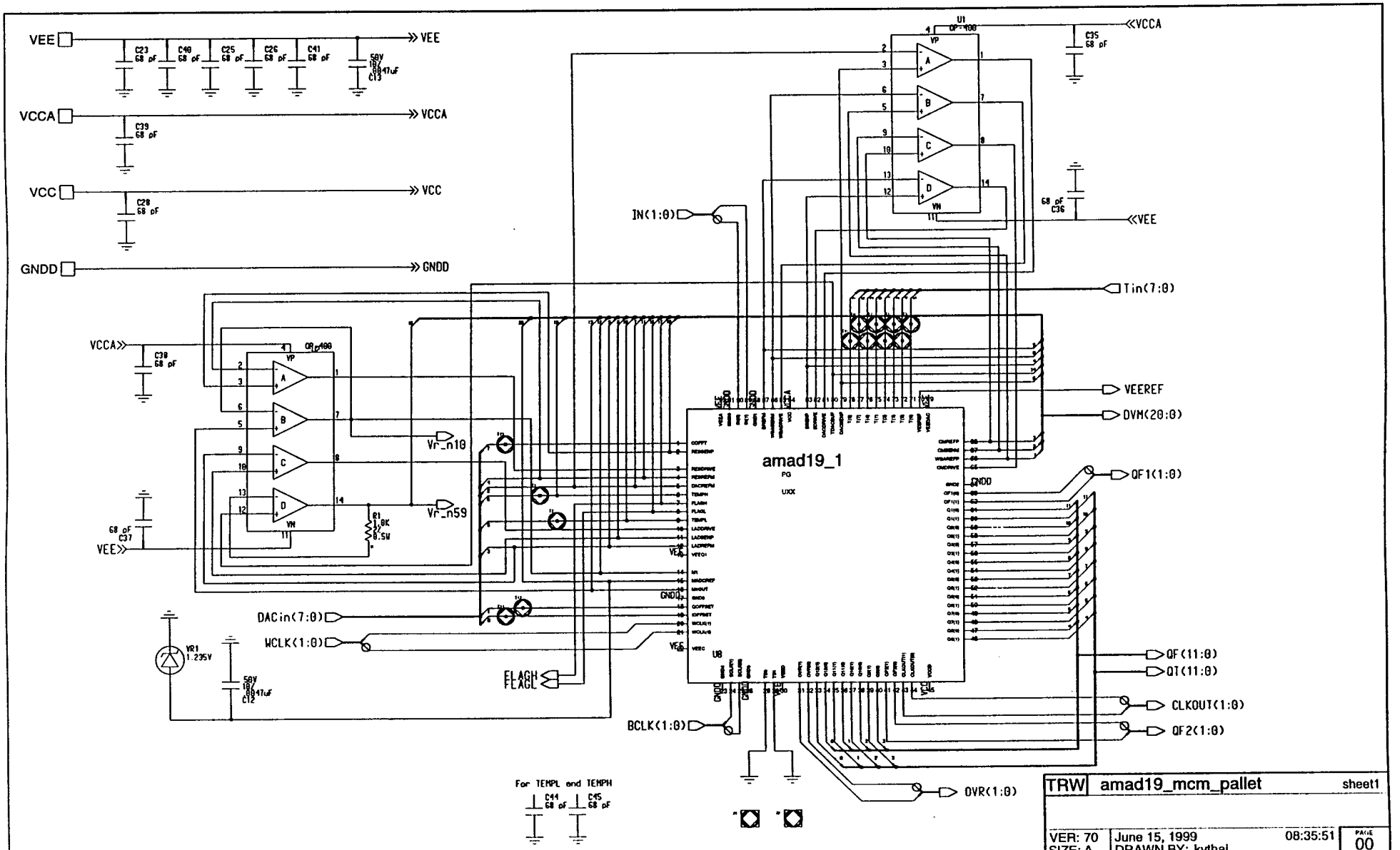
TRW HSAD9
S/N: 061099

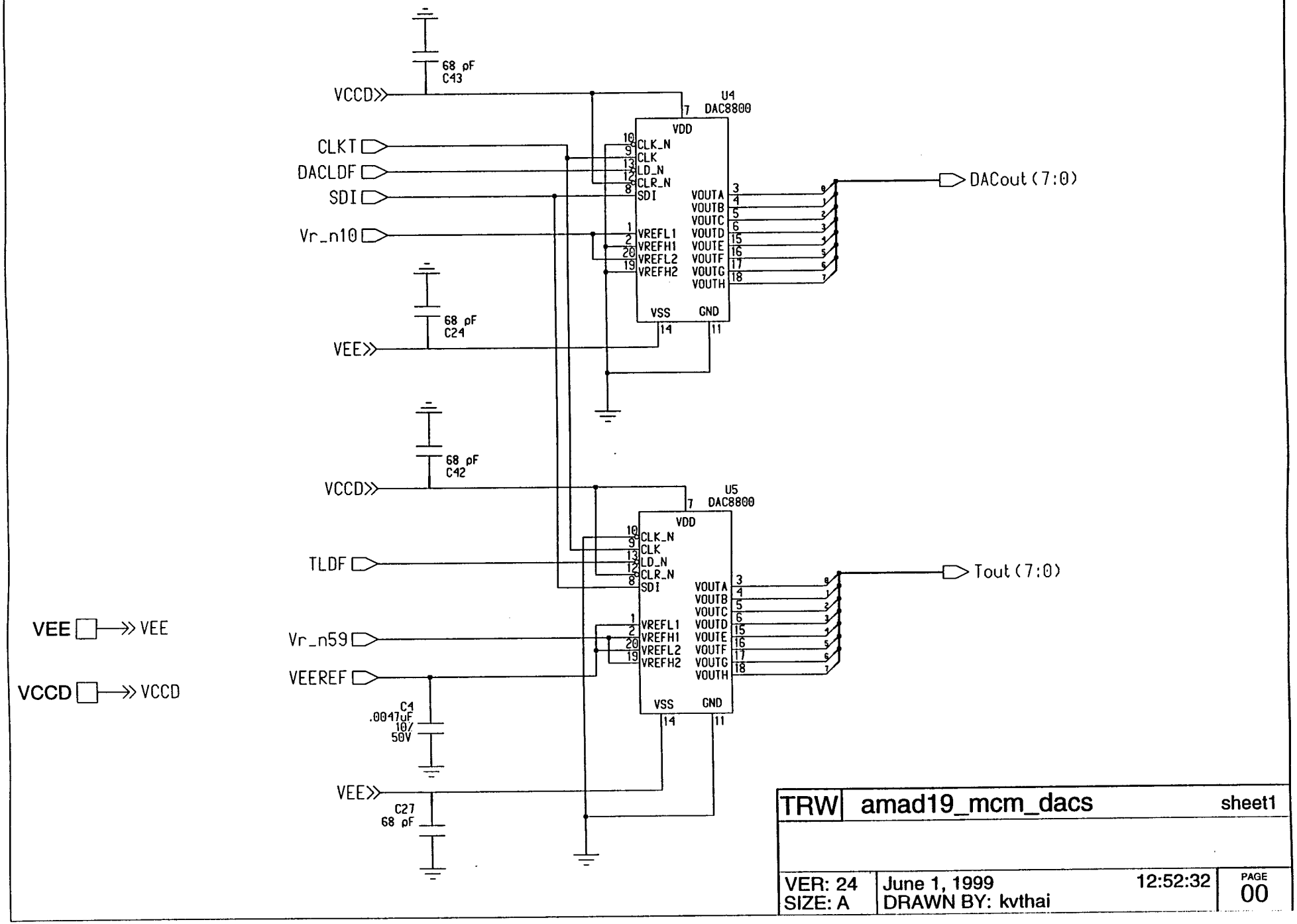
Cutout on Layers 1 - 7

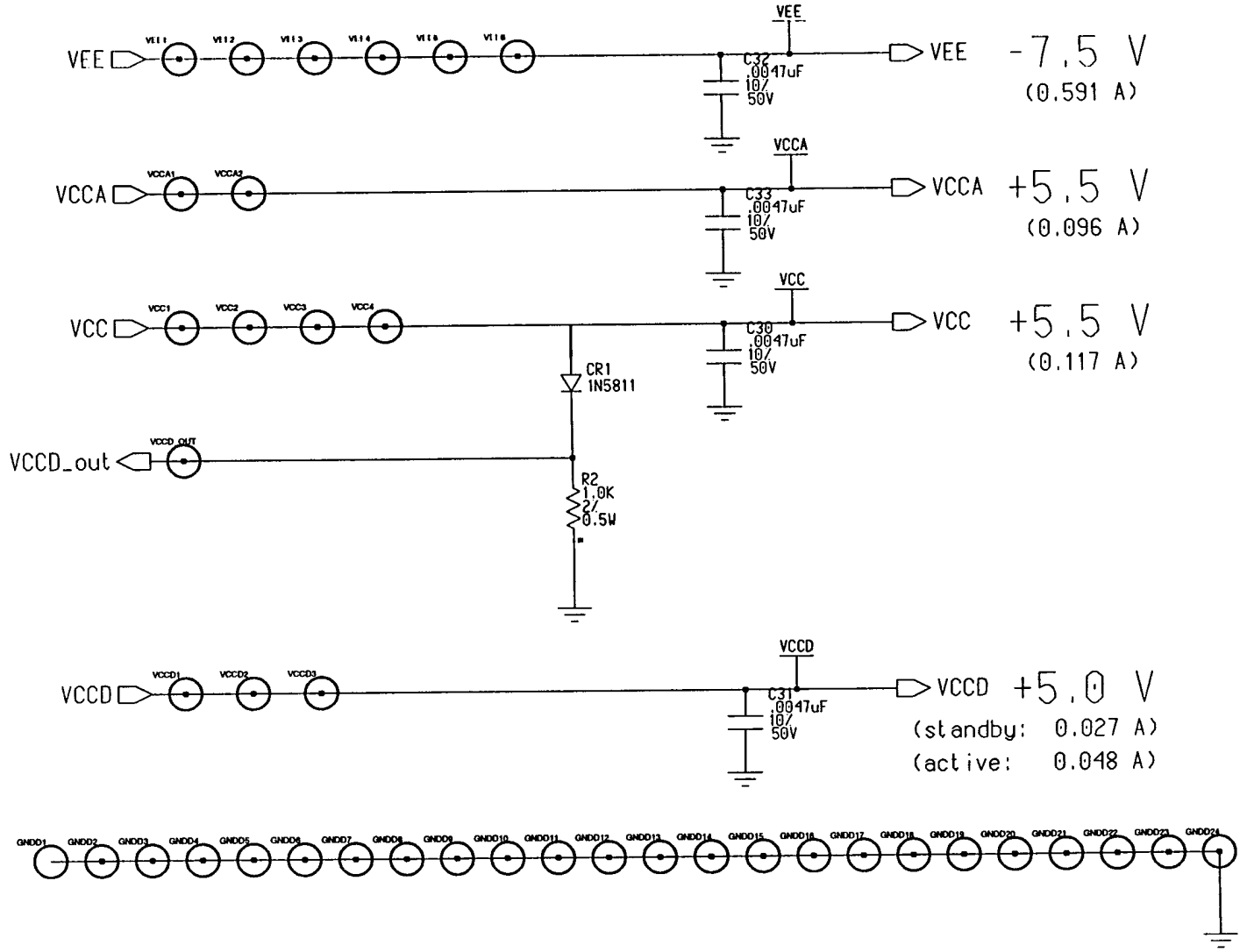


SILKSCREEN_1: LAYER_2, SIGNAL_1 (HSAD9 MCM)

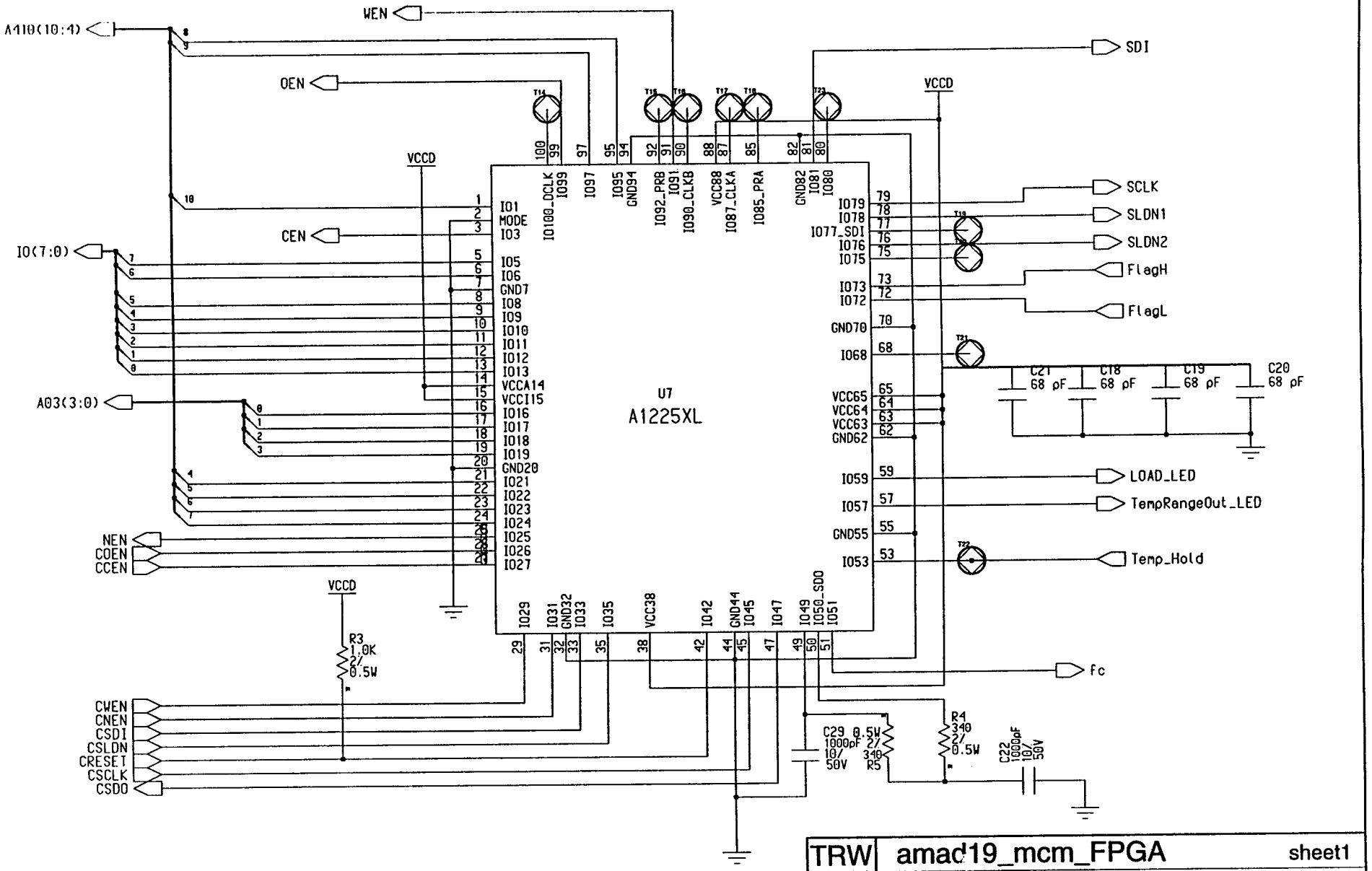

WCLK(1)
WCLK(0)
BCLK(1)
BCLK(0)
C14 .1uF dcblock
C15 .1uF dcblock
IN(1)
IN(0)
C16 .1uF dcblock
amad19_mcm_pallet
U1
amad19_mcm_dvm
U5
amad19_mcm_data
U6
amad19_mcm_dacs
U2
amad19_mcm_FPGA
U4
COEN
CCEN
CWEN
CNEN
CSDI
CSCLK
CSLDN
CReset
CSDO
Temp_Hold
amad19_mcm_power_conn
U3
VCCD_out
VEE
VCCA
VCC
VCCD
U9
X2C0C16
CE_N
OE_N
WE_N
MC_N
AS_N
VCCD
C34
.68 uF
Fc_1MHz
LOAD_LED
TempRangeOut_LED
TRW
amad19_mcm
sheet1
HSAD9 MCM
VER: 126
SIZE: A
July 12, 1999
DRAWN BY: kvthal
09:24:46
PAGE
00


VEE
VCCA
VCC
GNDD
IN(1:0)
Tin(7:0)
VEEREF
DVM(20:0)
QF1(1:0)
QF(11:0)
QT(11:0)
CLKOUT(1:0)
QF2(1:0)
OVR(1:0)
DACin(7:0)
WCLK(1:0)
BCLK(1:0)
FLAGH
FLAGL
Vr_n10
Vr_n59
amad19_1
PG
UXX
U8
U1
VR1
1.235V
For TEMPL and TEMPH
TRW
amad19_mcm_pallet
sheet1
VER: 70
SIZE: A
June 15, 1999
DRAWN BY: kvthai
08:35:51
PAGE
00

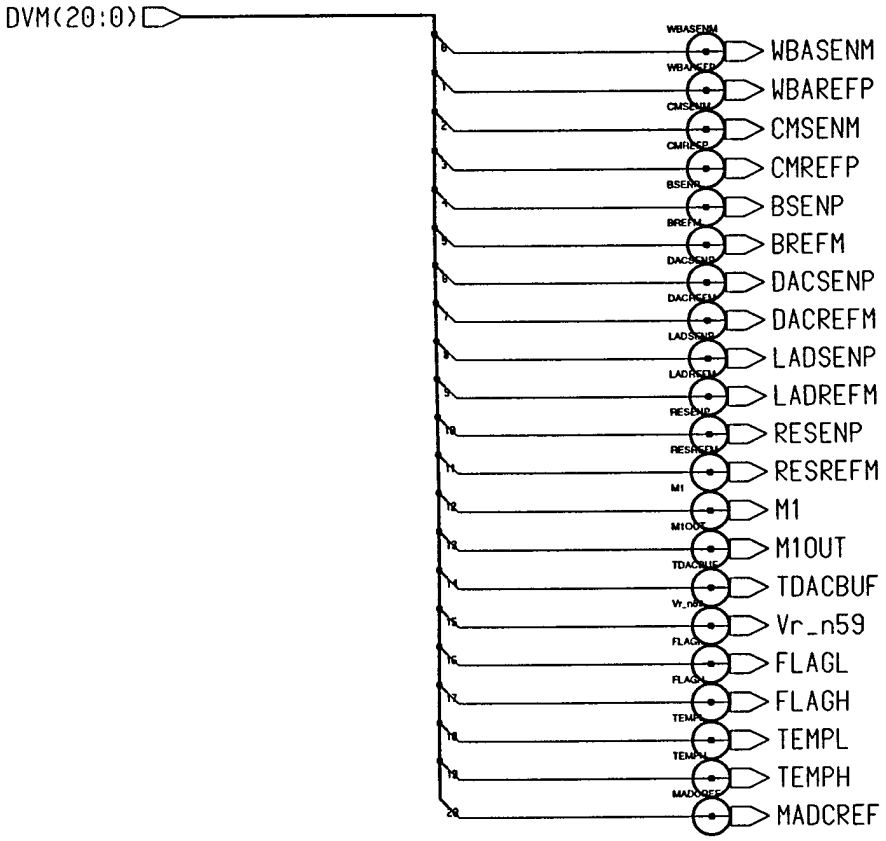

68 pF
C43
VCCD
U4
DAC8800
VDD
CLK_N
CLK
LD_N
CLR_N
SDI
VREFL1
VREFH1
VREFL2
VREFH2
VOUTA
VOUTB
VOUTC
VOUTD
VOUTE
VOUTF
VOUTG
VOUTH
VSS
GND
CLKT
DACLDF
SDI
Vr_n10
DACout(7:0)
68 pF
C24
VEE
68 pF
C42
VCCD
U5
DAC8800
TLDF
Tout(7:0)
VEE
VEE
VCCD
VCCD
Vr_n59
VEEREF
C4
.0047uF
10/
50V
VEE
C27
68 pF
TRW
amad19_mcm_dacs
sheet1
VER: 24
SIZE: A
June 1, 1999
DRAWN BY: kvthai
12:52:32
PAGE
00



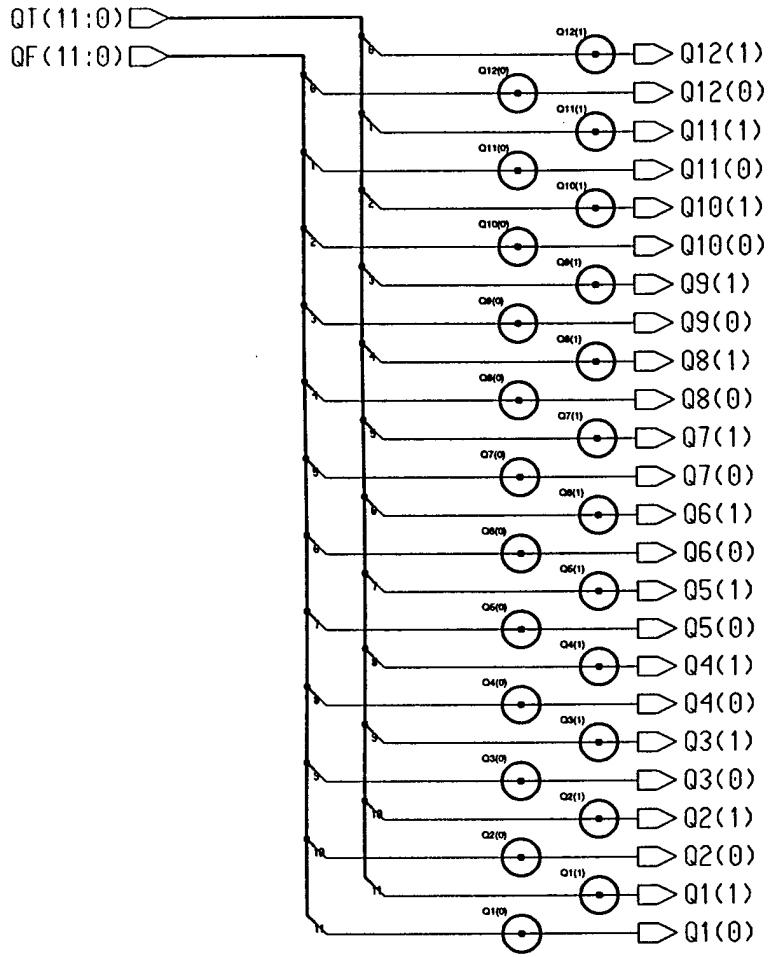
TRW	amad19_mcm_power_conn	sheet1
VER: 46 SIZE: A	May 25, 1999 DRAWN BY: kvthai	18:25:31
		PAGE 00

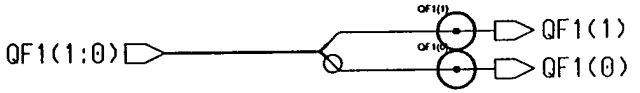


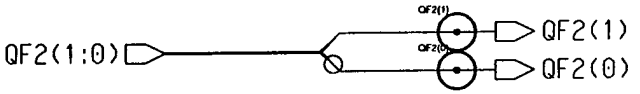
TRW	amad19_mcm_FPGA	sheet1
VER: 33 SIZE: A	July 12, 1999 DRAWN BY: kvthai	09:16:55
PAGE 00		

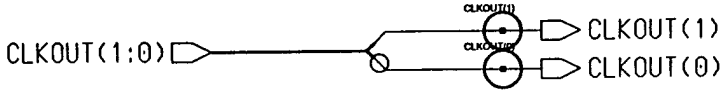


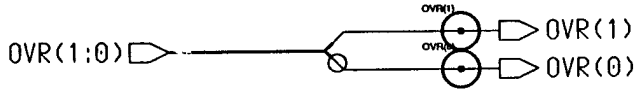
TRW	amad19_mcm_dvm		sheet1
VER: 17 SIZE: A	July 12, 1999 DRAWN BY: kvthai	11:32:43	PAGE 00







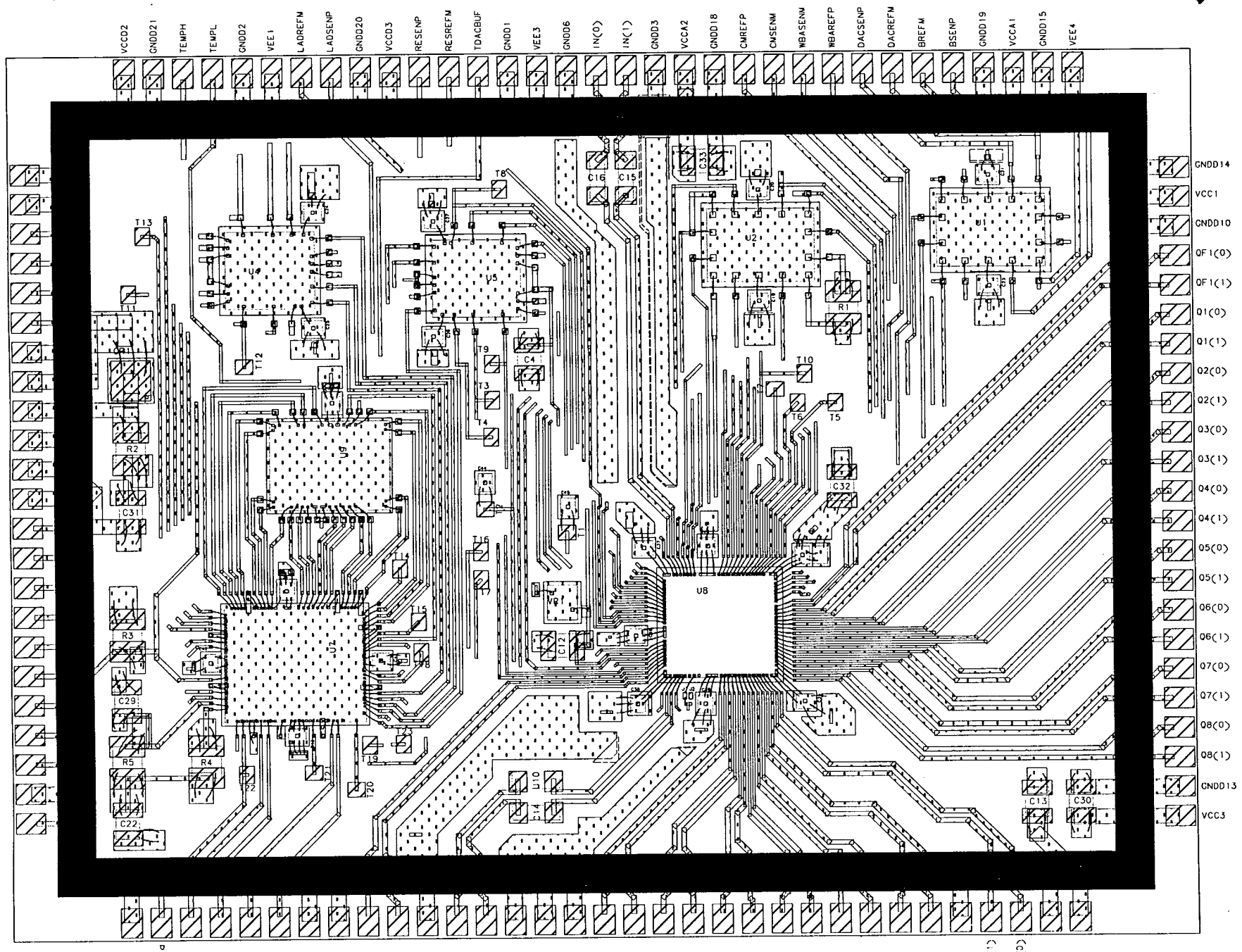




TRW	amad19_mcm_data	sheet1
VER: 14 SIZE: A	May 5, 1999 DRAWN BY: kvthai	13:44:53
		PAGE 00

MCM Station BOM file

ITEM_NUMBER	PART NO.	ALT. PART NO.	COUNT	DESCRIPTION	REFERENCE	SOURCE
1	1A036-337	1A074-561Z-001	7	CAP (4700pF) size AA	C4 C12 C13 C30 C31 C32 C33	ESS
2	1A036-336	1A074-557Z-001	2	CAP (1000pF) size AA	C22 C29	ESS
3	1DA29-002	1N5811	1	1N5811	CR1	
4	1K070-073	1K055-248W-001	3	RES (1K)	R1 R2 R3	
5	1K070-074	1K055-236W-001	2	RES (340)	R4 R5	
6	A1225XL-VQ100C	a1225xl	1	A1225XL	U7	
7	DAC8800	dac8800	2	DAC8800	U4 U5	
8	LM185H-2.5	lm385	1	LM185	VR1	
9	OP400AY	op400	2	OP-400	U1 U2	
10	amad19_1	amad19_1	1	amad19_1	U8	
11	dcblock	dcblock	4	dcblock	C14 C15 C16 U10	
12	dicap	dicap	22	dicap	C18 C19 C20 C21 C23 C24 C25 C26 C27 C28 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45	
13	x20c16	x20c16	1	x20c16	U9	
14	jumperpad	jumperpad	2	jumperpad	J1 J2	
15	padout	padout	112	padout		
16	testpt	testpt	23	probe pads	T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22 T23	


VCCD2
GNDD21
TEMPH
TEMPL
GNDD2
VEE1
LADREFN
LADSENP
GNDD20
VCCD3
RESENP
RESREFM
TDACBUF
GNDD1
VEE3
GNDD6
IN(0)
IN(1)
GNDD3
VCCA2
GNDD18
CMREFP
CMSENM
WBASENM
WBAREFP
DACSENP
DACREFM
BREFM
BSENP
GNDD19
VCCA1
GNDD15
VEE4
VEE2
GNDD12
M1OUT
M1
Vr_n59
MADCREF
GNDD9
VCC4
VCCD_OUT
GNDD16
VCCD1
GNDD7
COEN
CCEN
CWEN
CNEN
CSDI
CSLDN
CReset
CSCLK
CSDO
GNDD22
fc_1MHz
GNDD14
VCC1
GNDD10
OF1(0)
OF1(1)
Q1(0)
Q1(1)
Q2(0)
Q2(1)
Q3(0)
Q3(1)
Q4(0)
Q4(1)
Q5(0)
Q5(1)
Q6(0)
Q6(1)
Q7(0)
Q7(1)
Q8(0)
Q8(1)
GNDD13
VCC3
GNDD5
Temp_Hold
TRG_LED
_LED
FLAGL
FLAGH
VEE5
GNDD17
WCLK(1)
WCLK(0)
GNDD8
BCLK(1)
BCLK(0)
GNDD24
VCC2
GNDD23
OVR(1)
OVR(0)
D12(1)
D12(0)
D11(1)
D11(0)
D10(1)
D10(0)
D9(1)
D9(0)
D8(1)
D8(0)
GNDD4
VEE6
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
R1
R2
R3
R4
R5
C4
C12
C13
C14
C15
C16
C22
C29
C30
C31
C32
C33
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T12
T13
T15
T16
T20